PRELMINARY

INTEGRATED COLOR SPACE / RASTER-TO-BLOCK CONVERTER

FEATURES

- Raster-to-block and block-to-raster conversions with strip buffer of external SRAMs.
- Color space conversions of RGB to/from YCbCr or YeMaCy.
- Supports Fast Preview expansion and Lossless Compression/Expansion modes of the ZR36050.
- Exclusive dual pixel buses. Separate format and color space conversions on the ZR36050 data and output data during compression and expansion.
- Supports 4:4:4, 4:4:4:4, 4:2:2, 4:1:1 and 1:0:0 I/O formats.
- Supports many format conversions between pixel input bus and pixel output bus, pixel input bus and ZR36050, and ZR36050 and pixel output bus.
- Supports filtering for image format conversions.
- Horizontal decimation/interpolation with optional filtering and vertical decimation/interpolation by line dropping or replication.
- Enable function of pixel I/O buses for asynchronous applications.
- Sequential processing mode simplifies motion JPEG implementation.
- Provides windowing function to select processing area.
- TTL levels for Input/Output.
- 160 pin PQFP.

DESCRIPTION

The ZR36016 is a pre- and post-processor for use with a ZR36050 JPEG Image Codec, performing raster-to-block reordering and color space conversion.

The ZR36016 accepts input pixels in a variety of common color spaces. The pixel data can undergo format and color space conversion, with converted data available on the pixel output bus (Figure 1). When compressing, the data fed to the ZR36050 can be cropped within a selected window area, and its format can be different from that of the pixel output bus. For instance, it is possible to output an RGB(4:4:4) input onto the pixel output bus and to feed the ZR36050 with a YbCr(4:2:2) format. It is also possible to output a YCbCr(4:2:2) format input as RGB(4:4:4) and to feed the ZR36050 with a YCbCr(4:1:1) format. During expansion, for instance, the ZR36016 can output an RGB(4:4:4) input directly onto the output pixel bus, and after converting YCbCr(4:2:2) format coming from the ZR36050 into RGB(4:4:4), it overlays it in a window on the pixel input data.

The ZR36016 uses an external SRAM double-strip buffer for raster-block conversions and block interleaving. The Fast Preview and Lossless modes of operation of the ZR36050 are also supported, in which case the SRAM is used only for raster-to-raster buffering and pixel interleaving. Depending on the SRAM size and the mode of operation, the maximum line length can be up to 64K pixels. The number of lines per image can be up to 64K.

Processing of data on the pixel buses can be continuous as required for live frame capture or Motion JPEG, or it can be discontinuous, with pixels transferred only when enabled by an enable signal.

The data transfer rate with the ZR36050 is at a maximum of 30 MHz, the system clock rate. The pixel buses transfer at a maximum of 30 MHz for 4:0:0, or at a frequency ratio of 1, 1/2 or 1/4 of the system clock for the other formats, depending on the format conversions that are selected.

As shown in Figure 2, the input pixel data pass through a multiplexer, to the color space convertor. In compression, this multiplexer always passes the pixel data (the top input). The output of the color space convertor takes two paths in compression, one to the pixel output bus and the other to the raster to block convertor. The data on each path can independently undergo format conversion, which in this context means a resolution transformation by decimation or interpolation, of the chrominance components; for example, decimation from

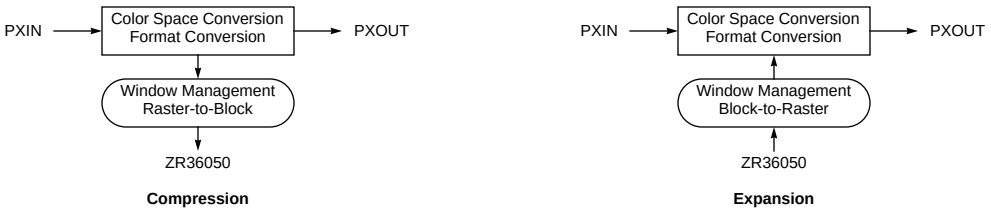


Figure 1. ZR36016 Operations with a ZR36050

YCrCb(4:4:4) to YCrCb(4:2;2). Format convertor #2 can perform decimation or interpolation of chrominance, while format convertor #1 can perform decimation in compression. In addition, data passing through format convertor #1 to the raster to block convertor can be decimated globally by 2, vertically and/or horizontally, to implement half-screen or quarter-screen compression.

In expansion, format convertor #2 can perform global horizontal and/or vertical interpolation, as well as interpolation of chrominance components. Its output is multiplexed with the pixel input bus, so that the pixel output bus contains the expanded data within a window on the input data. The color space convertor is switched in or out as required, simultaneously with the multiplexing of its input, so that the color space of the expanded data is independent of that of the input.

By means of the delay element shown, the processing pipeline delay from pixel input to output is kept constant even when color space conversion is bypassed. The input horizontal and vertical synchronization signals are output after undergoing an identical delay.

The mode of operation of the ZR36016 and operating parameters are determined by the control registers, which are programmed from the host interface. There are two modes of controlling compressions and expansions: single frame mode and sequential mode. In the single frame mode, the ZR36016 performs the desired process on a single frame (or field in case of interlaced motion video) and goes idle until explicitly commanded to perform another process. In sequential mode, a new process starts automatically every frame or field if enabled. The sequential mode is most suitable for motion JPEG.

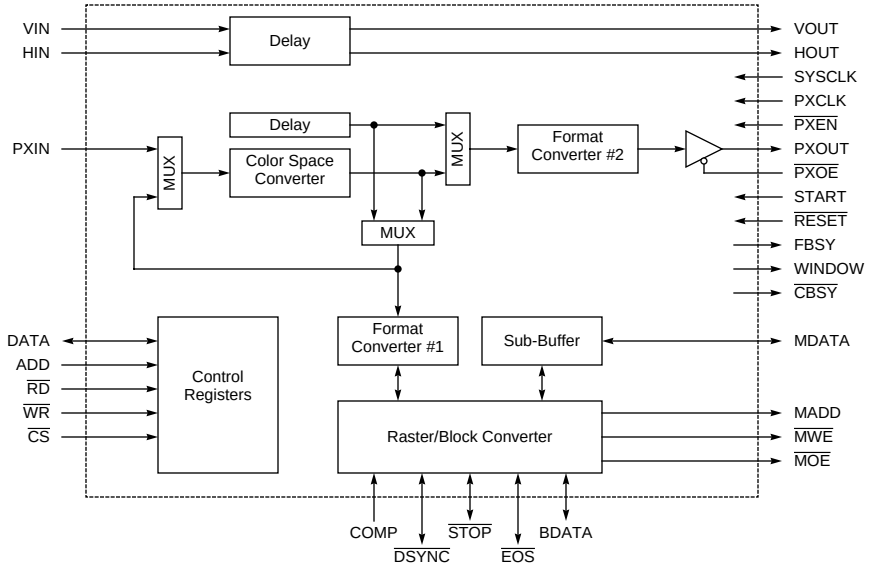


Figure 2. ZR36016 Block Diagrams

SIGNAL DESCRIPTIONS

Table 1: PIXEL Input/Output

Signal	I/O	Description
PXIN[23:0]	I	Pixel data input bus.
PXOUT[23:0]	O	Pixel data output bus.
$\overline{\text{PXOE}}$	I	PXOUT bus output enable.
HIN	I	Horizontal input data enable. Rising edge indicates beginning of scan line and start of NAX and PAX counts. For synchronization of PXIN.
VIN	I	Vertical input data enable. Rising edge indicates beginning of picture and start of NAY and PAY counts. For synchronization of PXIN.
HOUT	O	Horizontal output data enable. Follows HIN by internal processing delay. For synchronization of PXOUT.
VOUT	O	Vertical output data enable. Follows VIN by internal processing delay. For synchronization of PXOUT.
$\overline{\text{PXEN}}$	I	Pixel enable for PXIN and PXOUT. For discontinuous transfers.

Table 2: Host Interface

Signal	I/O	Description
ADD[1:0]	I	Internal registers address input.
DATA[7:0]	I/O	Internal registers data bus.
$\overline{\text{WR}}$	I	Write enable to internal registers. Written to on rising edge.
$\overline{\text{RD}}$	I	Read enable for internal registers.
$\overline{\text{CS}}$	I	Chip select for host interface.
$\overline{\text{CBSY}}$	I	CODEC busy. Indicates that the pixel side is ready to exchange strip buffers, but the ZR36050 side is not ready yet.

Table 3: Strip Buffer Memory Interface

Signal	I/O	Description
MDATA[15:0]	I/O	Memory data bus for strip buffer.
MADD[15:0]	O	Memory address for strip buffer.
$\overline{\text{MWE}}$	O	Memory write enable for strip buffer.
$\overline{\text{MOE}}$	O	Memory output enable for reading strip buffer.

Table 4: ZR36050 Interface

Signal	I/O	Description
BDATA[7:0]	I/O	Block data bus, connected to ZR36050 PIXEL bus.
$\overline{\text{DSYNC}}$	I/O	Block data synchronization with ZR36050.
$\overline{\text{STOP}}$	I/O	Data flow control with ZR36050.
$\overline{\text{EOS}}$	I/O	End of scan control with ZR36050.
COMP [1]	I	Compression/expansion mode indicator from ZR36050.

1. The state of the COMP pin determines the direction of the bidirectional pins BDATA, $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, and $\overline{\text{EOS}}$. When COMP is high (the ZR36050 is in compression mode), BDATA, $\overline{\text{DSYNC}}$ and $\overline{\text{EOS}}$ are outputs and $\overline{\text{STOP}}$ is an input. When COMP is low (the ZR36050 is in expansion mode), BDATA, $\overline{\text{DSYNC}}$ and $\overline{\text{EOS}}$ are inputs and $\overline{\text{STOP}}$ is an output.

Table 5: System Interface

Signal	I/O	Description
WINDOW	O	Indicates data is within window area.
FBSY	O	Frame busy. Indicates processing of frame.
START	I	Starts processing with the rising edge in single frame mode, or enables sequential mode.
SYSCLK	I	System clock. ZR36050 bus is synchronous with this clock.
PXCLK	I	Pixel clock. HIN, VIN and PXIN are synchronous with this clock on input. HOUT, VOUT, PXOUT and WINDOW are synchronous with this clock on output.
$\overline{\text{RESET}}$ [1]	I	Initial hard reset. Must be held low for 8 SYSCLK cycles. Internal state remains reset for two sysclk cycles after releasing $\overline{\text{RESET}}$.

1. When $\overline{\text{RESET}}$ is active, HOUT, VOUT, $\overline{\text{CBSY}}$, $\overline{\text{MWE}}$ and $\overline{\text{MOE}}$ are driven high, WINDOW, FBSY and MADD are driven low, PXOUT is unaffected (depends on PXIN and $\overline{\text{PXOE}}$ as usual), DATA is unaffected (depends on $\overline{\text{CS}}$ and $\overline{\text{RD}}$ as usual), and BDATA, $\overline{\text{DSYNC}}$, $\overline{\text{STOP}}$, and $\overline{\text{EOS}}$ depend on COMP as usual.

FUNCTIONAL DESCRIPTION

Control Registers

The internal control registers of the ZR36016 are shown in Figure 3. The access to these registers is through the host interface. Access to the Mode, Address Pointer and Configuration Tables is possible only when the ZR36016 is idle or when FBSY is not asserted. However, it is always possible to access the GO/STOP register.

There are four byte-wide direct access registers and twelve byte-wide indirect access registers.

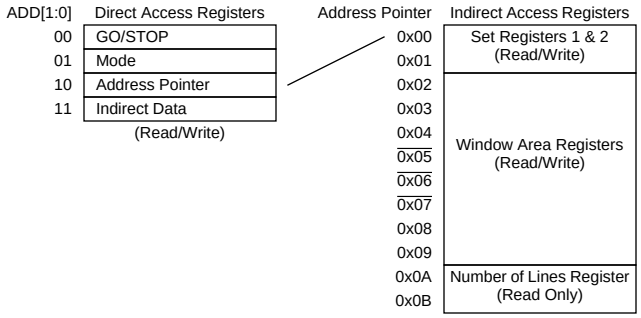


Figure 3. Control Registers

Access to the indirect registers uses the Address Pointer direct register. Its loaded value is used to point to the location from which accesses start in the indirect registers. For example, to write starting from the top of the Window Area Registers section, write 0x02 in the Address Pointer register and after that write the data in the Indirect Data register. After the first write to the Address Pointer register, the address pointer is incremented automatically after each access of the Indirect Data register. The Address Pointer register stops incrementing at 0x0B, even if the host continues to access the Indirect Data register.

GO/STOP Register

Read/Write Direct address: 0x00

Initial Value 0x00

Function Register to enable and stop processing by the ZR36016.

7	6	5	4	3	2	1	0
Version Number				–	–	–	GO/STOP

Bit 0 **GO/STOP**: Processing enable and stop bit.

Initial value = 0.

0= Terminates the processing.

1= Enables processing.

A 1 in the GO/STOP bit, in concert with the START signal, enables processing by the ZR36016. Once the GO/STOP bit has been set, processing will be enabled when START is high. For compression the actual processing period starts with the following rising edge of VIN and for expansion with the first $\overline{\text{DSYNC}}$. Clearing the GO/STOP bit at any time prevents the start of any future processing.

In the single frame mode the GO/STOP bit is cleared automatically after the single frame has been processed, and it must be set again to process a new frame.

In the sequential mode, when GO is set it remains set but the processing period can be controlled with the START signal.

Bits 1-3 Reserved.

Bits 4-7 **Version Number:** The version number of the ZR36016.

These bits contain the version number. Values start at 0 and increment for each silicon step. Read only.

Mode Register

Read/Write Direct address: 0x01

Initial Value 0x91

Function Determines the basic operating modes and formats of the ZR36016.

7	6	5	4	3	2	1	0
CMPR	DSPY		MODE				

Bit 0-4 **MODE**: Determines the PXIN input and ZR36050 image formats and color spaces. Initial Value = 0x11.

MODE (HEX)	PXBIN Bus Image Format	PXBIN Bus Color Space	ZR36050 Image Format Input (Compression) Output (Expansion) Image Format	ZR36050 Image Format Input (Compression) Output (Expansion) Color Space
00	4:4:4	RGB	4:4:4	YCbCr
01			4:2:2	YCbCr
02			4:1:1 (H2V2)	YCbCr
03 [1]			4:0:0	Y Only
04			4:4:4	RGB
05~07	Reserved			
08	4:4:4	YCbCr	4:4:4	YCbCr
09			4:2:2	YCbCr
0A			4:1:1 (H2V2)	YCbCr
0B [1]			4:0:0	Y Only
0C			4:4:4	RGB
0D~10	Reserved			
11	4:2:2	YCbCr	4:2:2	YCbCr
12			4:1:1 (H2V2)	YCbCr
13 [1]			4:0:0	Y Only
14, 15	Reserved			
16	4:1:1 (PHILIPS)	YCbCr	4:1:1 (H4V1)	YCbCr
17 [1]			4:0:0	Y Only
18	Reserved			
19	4:4:4:4	–	4:4:4:4	–
1A	Reserved			
1B	1:0:0	–	1:0:0	–
1C~1F	Reserved			

1. For Compression Only. If programmed for expansion, then MODE = 0x16 is assumed.
2. RGB becomes YeMaCy when selected by the YMCS bit in Setup Register 2.
3. MODE = 0x16 and 0x17 are the Philips 4:1:1 format. Input and output pixel data use the upper 12 bits of PXIN and PXOUT buses.
4. 4:1:1(H4V1) refers to a format in which the Cb and Cr are decimated by 4 horizontally. 4:1:1(H2V2) refers to a format in which the Cb and Cr are decimated by 2 horizontally and 2 vertically (sometimes known as 4:2:0 format).
5. The image format conversions implied by this table are performed by Format Converter #1 in the block diagram.

Mode Register (Continued)

Bits 5-6 DSPY: Determines the PXOUT bus output formats.

Initial Value = 0x00.

Setting this field of the Mode register selects the output data format of the PXOUT bus, for each format of the PXIN bus as selected by the MODE field of the register, as shown in the table below.

DSPY Bit 6	DSPY Bit 5	PXIN Bus Image Format [1] 4:4:4 (RGB)	4:4:4 (YCbCr)	4:2:2 (YCbCr)	4:1:1 (Philips)	1:0:0	4:4:4:4
0	0	PXOUT is 4:4:4 (RGB)			PXOUT is 4:1:1 (Philips)	PXOUT is 1:0:0	PXOUT is 4:4:4
0	1	PXOUT is 4:4:4 (YCbCr)					
1	0	PXOUT is 4:2:2 (YCbCr)					
1	1	Reserved					

1. The image format conversions implied by this table are performed by Format Converter #2 in the block diagram.

Bit 7 CMPR: Selects compression or expansion

Initial Value = 1
0 = Expansion Mode.
1 = Compression Mode.

Setup Register 1

Read/Write Indirect address: 0x00

Initial Value 0x01

7	6	5	4	3	2	1	0
CKRT	VERT	HORZ	HRFL	DSFL	SBFL	RSTR	CNTI

Bit 0 **CNTI**: Single-Frame/Sequential processing selection.

Initial value = 1.

0= Single Frame Mode. Processes the image enabled by VIN and then enters an idle state. For processing still images.

1= Sequential Mode. Processes sequential images indefinitely, each VIN. For Motion JPEG.

Bit 1 **RSTR:** Transparent mode selection, for raster/raster conversion.

Initial Value = 0.

0= Selects the raster-to-block or block-to-raster conversion mode.

1= Selects the transparent raster-to-raster mode.

For the Fast Preview lossless compression/expansion functions of the ZR36050. The image formats supported, as set by the MODE field, are 4:4:4:4, 4:4:4, 4:2:2, or 4:1:1 (H4V1) (with pixel interleave). As the ZR36050 performs 1-D lossless only, the setting of RSTR = 1 in 4:1:1(H2V2) format is not permitted.

Note: The strip buffer processing delay is the same for both modes.

Setup Register 1 (Continued)

Bit 2 **SBFL:** Image format conversion filter.

Initial Value = 0.

0= Selects simple decimation or interpolation without filtering.

1= Selects decimation or interpolation of color components with filter processing.

This bit controls filtering in Format Converter #1.

Bit 3 **DSFL:** PXIN/OUT bus data image format conversion filter.

Initial Value = 0.

0= Selects simple decimation or interpolation without filtering.

1= Selects decimation or interpolation of color components with filter processing.

This bit controls filtering in Format Converter #2.

Bit 4 **HRFL:** Half-size horizontal decimation or interpolation filter.

Initial Value = 0.

0= Selects simple half-size horizontal decimation or interpolation without filtering.

1= Selects decimation or interpolation with filtering. Must be used only with HORZ = 1.

Bit 5 **HORZ:** Half-size horizontal decimation or interpolation.

Initial Value = 0.

0= Selects no horizontal decimation nor interpolation.

1= Selects half-size horizontal decimation on compression, and interpolation on expansion. The decimated data stream is loaded in the strip buffer on compression, and the data before interpolation is loaded on expansion. The decimation and interpolation are performed on Y, Cr and Cb, or on Y only, depending on the MODE field.

Bit 6 **VERT:** Half-size vertical decimation or interpolation.

Initial Value = 0.

0= Selects no vertical decimation nor interpolation.

1= Selects half-size vertical decimation (by line dropping) in compression or interpolation by line replication in expansion. The decimated data stream is loaded in the strip buffer on compression, and the data before interpolation is loaded on expansion. The lines dropped in decimation are the second, fourth,… lines of the active window. This bit does not apply to the 4:1:1(H2V2) format.

Bit 7 **CKRT:** Ratio of PXCLK to SYSCLK frequency, with half-size horizontal decimation/interpolation.

Initial Value = 0.

0= Selects normal PXCLK to SYSCLK frequency ratio when HORZ = 1.

1= Selects slow SYSCLK (doubles the PXCLK to SYSCLK frequency ratio) when HORZ = 1.

This bit selects the PXCLK to SYSCLK frequency ratio, when HORZ = 1 (horizontal half-size mode). It optionally allows the SYSCLK rate to be halved relative to its rate with full horizontal size. See Table 8.

Setup Register 2

Read/Write Indirect address: 0x01

Initial Value 0x00

7	6	5	4	3	2	1	0
–	SYEN	–	–	–	CCIR	SIGN	YMCS

Bit 0 **YMCS:** RGB or YeMaCy selection.

Initial Value = 0.

0= RGB.

1= YeMaCy. The ZR36016 treats RGB as YeMaCy when the image format on the PXIN/PXOUT buses are RGB in the MODE field.

Bit 1 **SIGN:** Signed values of Cr and Cb.

Initial Value = 0.
Selects the sign convention of Cr and Cb on the PXIN bus input and the output on the PXOUT bus.

0= Offset binary (unsigned).

1= 2's complement signed.

The data transfers with the ZR36050 are always unsigned. This bit is not used when MODE = 0x19 (4:4:4:4).

Bit 2 **CCIR:** CCIR signal level selection. Initial Value = 0. When the color space conversion is done, the signal levels can be as specified in CCIR601 or full scale. This bit is not used when MODE = 0x19 (4:4:4:4).

0= 8 bits full scale.

1= CCIR R601.2 standard levels.

Bit 3-5 **Reserved.**

Bit 6 **SYEN:** Function selection for $\overline{\text{PXOE}}$.

Initial Value = 0.

0= Tri-stating of PXOUT bus, HOUT and VOUT are controlled by $\overline{\text{PXOE}}$.

1= Only the PXOUT bus is three-stated by $\overline{\text{PXOE}}$.

Bit 7 **Reserved.**

The NAX, PAX, NAY and PAY registers define the offset and dimensions of the active area. See also Figure 4.

Window Area Register NAX-Lo

Read/Write Indirect address: 0x02

Initial Value 0x00

7	6	5	4	3	2	1	0
NAX[7:0]							

Bits 0-7 **NAX(7:0):** The number of pixels from the rising edge of HIN to the starting point of the active window area (X-axis offset). Lower 8 bits.

Initial Value = 0.

Window Area Register NAX-Hi

Read/Write Indirect address: 0x03

Initial Value 0x00

7	6	5	4	3	2	1	0
–	–	–	NAX[12:8]				

Bits 0-4 **NAX(12:8):** The number of pixels from the rising edge of HIN to the starting point of the active window area (X-axis offset). Upper 5 bits.

Initial Value = 0.

The range of NAX(12:0) is 0 to 8191.

Window Area Register PAX-Lo

Read/Write Indirect address: 0x04

Initial Value 0xD0

7	6	5	4	3	2	1	0
PAX[7:0]							

Bits 0-7 **PAX(7:0):** The number of pixels of active window area on a line (X-axis dimension). Lower 8 bits.

Initial Value = 0xD0.

Window Area Register PAX-Hi

Read/Write Indirect address: 0x05

Initial Value 0x02

7	6	5	4	3	2	1	0
PAX[15:8]							

Bits 0-7 **PAX(15:8):** The number of pixels of active window area on a line (X-axis dimension). Upper 8 bits.

Initial Value = 0x02.

The acceptable range of values of PAX(15:0) depends on the mode of operation, as shown in Table 18. The logical value of PAX is the same as its literal value for all literal values up to and including 0xFFFE. Thus, the logical value for literal PAX = 0xFFFE (65534) is 65534 pixels. The logical value for literal PAX = 0xFFFF (65535) is 65536 pixels.

Window Area Register NAY-Lo

Read/Write Indirect address: 0x06

Initial Value 0x00

7	6	5	4	3	2	1	0
NAY[7:0]							

Bits 0-7 **NAY(7:0):** The number of lines from the rising edge of VIN to the starting point of the active window area (Y-axis offset). Lower 8 bits.

Initial Value = 0.

Window Area Register NAY-Hi

Read/Write Indirect address: 0x07

Initial Value 0x00

7	6	5	4	3	2	1	0
–	–	–	NAY[12:8]				

Bits 0-4 **NAY(12:8):** The number of lines from the rising edge of VIN to the starting point of the active window area (Y-axis offset). Upper 5 bits.

Initial Value = 0.

he range of NAY(12:0) is 0 to 8191.

Window Area Register PAY-Lo

Read/Write Indirect address: 0x08

Initial Value 0xF0

7	6	5	4	3	2	1	0
PAY[7:0]							

Bits 0-7 **PAY(7:0):** The number of lines of the active window area {Y-axis dimension]. Lower 8 bits.

Initial Value = 0xF0.

Window Area Register PAY-Hi

Read/Write Indirect address: 0x09

Initial Value 0x00

7	6	5	4	3	2	1	0
PAY[15:8]							

Bits 0-7 **PAY(15:8):** The number of lines of the active window area {Y-axis dimension]. Upper 8 bits.

Initial Value = 0x00.

The logical value of PAY is the same as its literal value for all literal values up to and including 0xFFFE. Thus, the logical value for literal PAY = 0xFFFE (65534) is 65534 pixels. The logical value for literal PAY = 0xFFFF (65535) is 65536 pixels. If PAY = 0 in compression, then the number of lines processed is determined by the active period of VIN. PAY (logical) must be an even number when vertical decimation/interpolation is used.

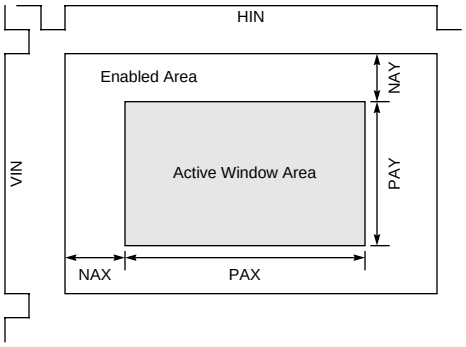


Figure 4. Active Window Area

Number Of Lines Register NOL-Lo

Read Only Indirect address: 0x0A

Initial Value PAY[7:0]

7	6	5	4	3	2	1	0
NOL[7:0]							

Bits 0-7 **NOL(7:0):** The actual number of lines that were processed in compression. Lower 8 bits.

Initial Value = PAY(7:0).

Number Of Lines Register NOL-Hi

Read Only Indirect address: 0x0B

Initial Value PAY[15:8]

7	6	5	4	3	2	1	0
PAY[15:8]							

Bits 0-7 **NOL(15:8):** The number of processed lines when compressing. Upper 8 bits.

Initial Value = PAY(15:8).

If PAY≠0, its logical value determines the number of lines actually processed in compression. If PAY = 0, the ZR36016 processes all lines input until the falling edge of VIN. If the number of lines input during the active period of VIN is not an exact multiple of the strip height (see Table 19), then the ZR36016 will abandon the incomplete strip. The NOL register will indicate only the number of lines actually processed.

In the sequential mode, the value read from this register is the number of lines processed in the previous VIN active interval.

If 65536 lines are processed, the value in NOL will be 0x0000. The ZR36016 can process a maximum of 65536 lines. If the number of lines exceeds 65536, then the ZR36016 terminates the processing after 65536 lines.

Register Summary

Table 6: Direct Registers

Name	Address	7	6	5	4	3	2	1	0
GO/STOP Register	0x00	Version Number				–	–	–	GO/STOP
Mode Register	0x01	CMPR	DSPY		MODE				
Address Register	0x02	Indirect Registers Address Pointer							
Indirect Data	0x03	Indirect Registers Data							

Table 7: Direct Registers

Name	Pointer	7	6	5	4	3	2	1	0
Setup Register 1	0x00	CKRT	VERT	HORZ	HRFL	DSFL	SBFL	RSTR	CNTI
Setup Register 2	0x01	–	SYEN	–	–	–	CCIR	SIGN	YMCS
NAX-Lo	0x02	NAX[7:0]							
NAX-Hi	0x03	–	–	–	NAX[12:8]				
PAX-Lo	0x04	PAX[7:0]							
PAX-Hi	0x05	PAX[15:8]							
NAY-Lo	0x06	NAY[7:0]							
NAY-Hi	0x07	–	–	–	NAY[12:8]				
PAY-Lo	0x08	PAY[7:0]							
PAY-Hi	0x09	PAY[15:8]							
NOL-Lo	0x0A	NOL[7:0]							
NOL-Hi	0x0B	NOL[15:8]							

Hardware Interfaces

Image Input/Outputs

SYSCLK and PXCLK

The ZR36016 requires two system clocks: PXCLK, at the data rate of the pixel buses, and SYSCLK, at the data rate of the ZR36050 interface. The frequency ratio of PXCLK to SYSCLK depends on the compressed image format and other setup register bits, as shown in Table 8.

For some of the configurations shown in the table, the PXCLK to SYSCLK frequency ratio is 1. When this happens, the output pixel bus, PXOUT, is actually clocked with SYSCLK. PXCLK, at the same rate as SYSCLK, is still required, however, to clock the input pixel bus PXIN, and for reset and other operations.

When the HORZ setup register bit is set, for horizontal decimation or interpolation, there are in most cases two options for the PXCLK to SYSCLK frequency ratio as selected by the CKRT bit of Setup Register 1.

Table 8: Ratio of PXCLK to SYSCLK

ZR36050 Image Format	HORZ			VERT	Compression Format and Resolution	PXCLK to SYSCLK Frequency Ratio	
	Bit	Decimation/ Interpolation [1]				CKRT	
		Y	CB/CR			0	1
4:2:2	1	◆	◆	1	2:1:1 (Quarter Screen)	1/2	1
4:2:2	1	◆	◆	0	2:1:1 (Horizontal Half-Screen)	1/2	1
4:2:2	0	–	–	1	4:2:2 (Vertical Half-Screen)	1/2	
4:2:2	0	–	–	0	4:2:2 (Full-Screen)	1/2	
4:1:1 (H4V1)	1	◆	–	1	2:1:1 (Quarter Screen)	1/2	1
4:1:1 (H4V1)	1	◆	–	0	2:1:1 (Horizontal Half-Screen)	1/2	1
4:1:1 (H4V1)	0	–	–	1	4:1:1 (Vertical Half-Screen)	1/2	
4:1:1 (H4V1)	0	–	–	0	4:1:1 (Full-Screen)	1/2	
4:1:1 (H2V2)	–	–	–	–	4:1:1 (Full-Screen)	1/2	
4:4:4	1	Each Component		1	2:2:2 (Quarter Screen)	1/4	1/2
4:4:4	1	Each Component		0	2:2:2 (Horizontal Half-Screen)	1/4	1/2
4:4:4	0	–	–	1	4:4:4 (Vertical Half-Screen)	1/4	
4:4:4	0	–	–	0	4:4:4 (Full-Screen)	1/4	
4:4:4:4	1	Each Component		1	2:2:2:2 (Quarter Screen)	1/2	1
4:4:4:4	1	Each Component		0	2:2:2:2 (Horizontal Half-Screen)	1/2	1
4:4:4:4	0	–	–	1	4:4:4:4 (Vertical Half-Screen)	1/2	
4:4:4:4	0	–	–	0	4:4:4:4 (Full-Screen)	1/2	
4:0:0 (1:0:0)	1	◆	–	1	2:0:0 (Quarter Screen)	1	
4:0:0 (1:0:0)	1	◆	–	0	2:0:0 (Horizontal Half-Screen)	1	
4:0:0 (1:0:0)	0	–	–	1	4:0:0 (Vertical Half-Screen)	1	
4:0:0 (1:0:0)	0	–	–	0	4:0:0 (Full-Screen)	1	

1. ◆ = Decimation/Interpolation is performed on these components; – = Not performed or not applicable.

PXIN/PXOUT Bus Data Arrangement

The PXIN/PXOUT buses are 24 bits each. The 24 bits are divided into 8-bit bytes, as follows.

	MSB LSB	MSB LSB	MSB LSB
PXIN/OUT[23:0]	23:16	15:8	7:0

The I/O arrangement is determined by the MODE and DSPY fields, as shown below in Table 9. In this table, the 3 components of (4:4:4), (4:2:2), (4:1:1), (1:0:0) formats are designated (A:B:C), components of (4:4:4:4) format are designated (A:B:C:D), and (A:B:C) corresponds with (R:G:B), (Y:Cb:Cr) or (Cy:Ma:Ye). 1st, 2nd, etc., refer to the PXCLK time slots.

Table 9: I/O Bus Arrangements

PXINOUT Bus	I/O Format											
	4:4:4		4:2:2		4:1:1				1:0:0		4:4:4:4	
	1st	2nd	1st	2nd	1st	2nd	3rd	4th	1st	2nd	1st	2nd
23-16	A	A	A	A	A	A	A	A	A	A	A	C
15-8	B	B	B	C	B[7:6] /C[7:6]	B[5:4] /C[5:6]	B[3:2] /C[3:2]	B[1:0] /C[1:0]	–	–	B	D
7-0	C	C	–	–	–	–	–	–	–	–	–	–

4:1:1 in Table 9 is the Philips H4V1 format. As shown in Table 10, it uses only the upper 12-bits on the PXIN/PXOUT buses.

Table 10: Philips 4:1:1 Format

PXIN/OUT	1st	2nd	3rd	4th
PXIN/OUT[23:16]	A[7:0]	A[7:0]	A[7:0]	A[7:0]
PXIN/OUT[15]	B[7]	B[5]	B[3]	B[1]
PXIN/OUT[14]	B[6]	B[4]	B[2]	B[0]
PXIN/OUT[13]	C[7]	C[5]	C[3]	C[1]
PXIN/OUT[12]	C[6]	C[4]	C[2]	C[0]
PXIN/OUT[11:0]	–	–	–	–

PXIN/PXOUT Delay

The image data which is input on the PXIN bus is output on the PXOUT bus after an internal delay which depends on the MODE field and HORZ bit of the registers. The delays of VIN to VOUT and HIN to HOUT are the same as these. See Table 11 and Figure 5.

Table 11: PXIN to PXOUT Delay

Configuration		Delay in PXCLK Clock Cycles (d)
MD [1]	HORZ	
0	0	20
0	1	24
1	0	17
1	1	20

1. Where MD = 1 when MODE = 0x0, 0x4, 0x8 or 0xC and = 0 for all others.

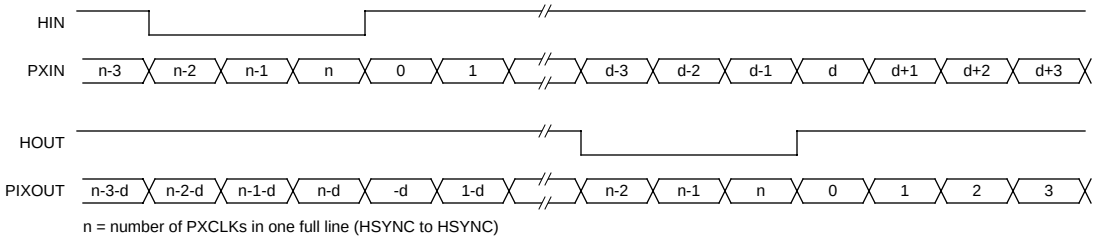


Figure 5. PXIN/PXOUT Delay Timing

Non-continuous I/O Using $\overline{\text{PXEN}}$

The pixel buses PXIN/PXOUT enter a freeze state when $\overline{\text{PXEN}}$ is not active. VIN and HIN must be used in a consistent manner as illustrated in Figures 10 and 11 when $\overline{\text{PXEN}}$ is used. VOUT, HOUT, PXOUT, WINDOW and FBSY are also affected by the freeze state but the ZR36050 interface and the strip buffer bus are always active, regardless of $\overline{\text{PXEN}}$.

To stop bus activity by entering the freeze state, $\overline{\text{PXEN}}$ must be not active for at least one PXCLK cycle, or when PXCLK = SYSCLK then it must be inactive for at least two PXCLK cycles. Proper operation is illustrated in the figures below for the various clock ratios.

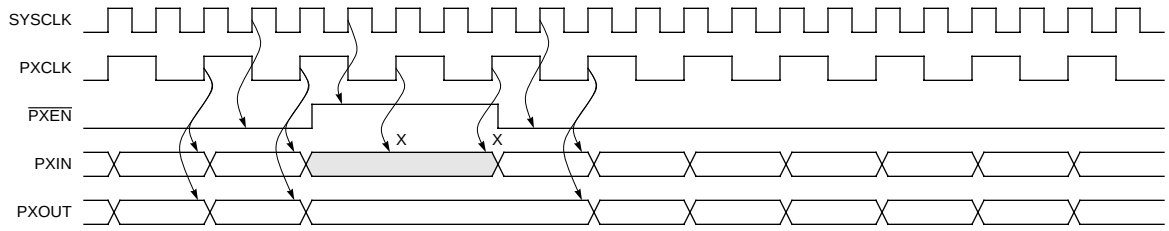


Figure 6. PXCLK = SYSCLK/2

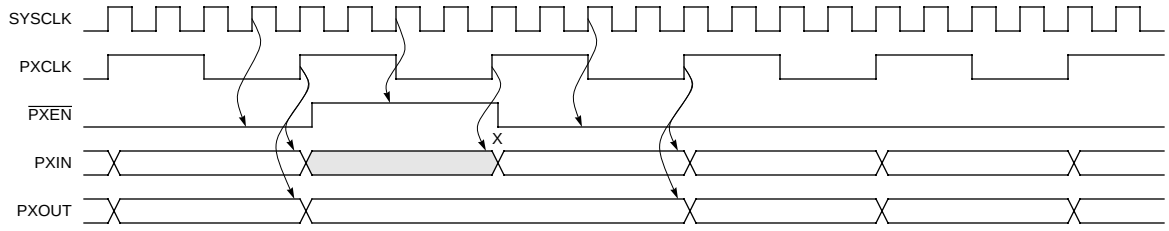


Figure 7. PXCLK = SYSCLK/4

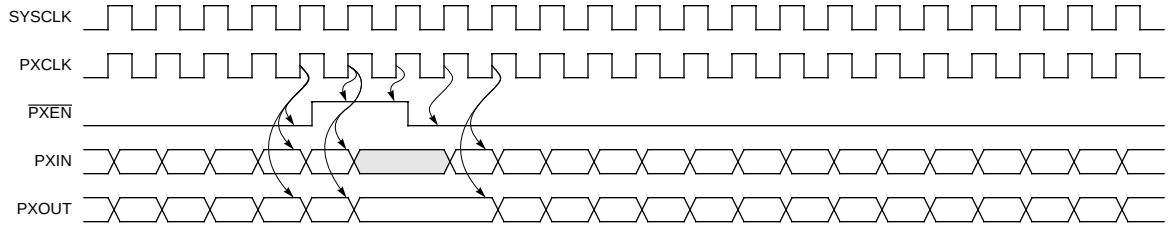


Figure 8. PXCLK = SYSCLK

Data Representation

The results of color space conversion are limited and rounded to 8 bits. These results may be output with the full 256 levels or reduced to 220 levels as specified by the CCIR R601.2 standard, by using the CCIR bit in Setup Register 2. The R,G,B and Y values are always unsigned, but offset binary or 2's complement representation may be selected for Cr and Cb signals by the SIGN bit. These choices are shown in Table 12 and Table 13.

Table 12: Data Representation With CCIR = 0

CCIR = 0		R, G, B, Y	Cr, Cb SIGN = 0	Cr, Cb SIGN = 1
Hex	Decimal	Unsigned	Offset Binary	2's Complement
0xFF	255	255	127	-1
0xFE	254	254	126	-2
:	:	:	:	:
0x81	129	129	1	-127
0x80	128	128	0	-128
0x7F	127	127	-1	127
:	:	:	:	:
0x01	1	1	-127	1
0x00	0	0	-128	0

Table 13: Data Representation With CCIR = 1

CCIR = 1		R, G, B, Y	Cr, Cb SIGN = 0	Cr, Cb SIGN = 1
Hex	Decimal	Unsigned	Offset Binary	2's Complement
0xFF	255			-1
0xFE	254			-2
:	:		112	:
0xF1	241	235		-15
0xF0	240		112	-16
:	:		:	:
0xEC	236		108	-20
0xEB	235	235	107	-21
:	:	:	:	:
0x91	145	145	17	-111
0x90	144	144	16	-112
:	:	:	:	
0x81	129	129	1	-112
0x80	128	128	0	
0x7F	127	127	-1	
:	:	:	:	112
0x70	112	112	-16	112
0x6F	111	111	-17	111
:	:	:	:	:
0x10	16	16	-112	16
0x0F	15			15
:	:			:
0x01	1	16	-112	1
0x00	0			0

HIN and VIN

The following restrictions must be observed for the HIN signal. The low interval (A in Figure 9) must be at least two PXCLK cycles. In addition the total period must be an even number of PXCLK cycles (B in Figure 9).

When $\overline{\text{PXEN}}$ is used to control the pixel data flow, the effective number of PXCLK cycles is modified. Effective cycles are counted only when $\overline{\text{PXEN}}$ is active, as illustrated in Figures 10 and 11.

The low interval of VIN must be at least 2 PXCLK cycles.

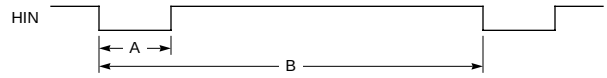


Figure 9. Restrictions for HIN

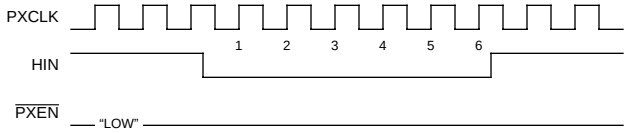


Figure 10. Effective PXCLK Cycles (6 Effective Cycles)

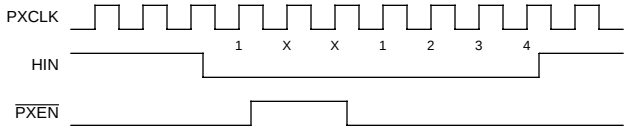


Figure 11. Effective PXCLK Cycles (4 Effective Cycles)

Decimation/Interpolation Filter Processing

Table 14 is a summary of the decimation and interpolation modes supported with the various compressed image formats. Table 15 shows the specific choices for each format as selected in the MODE field of the Mode Register. HORZ, VERT and CKRT are bits in Setup Register 1 that select the horizontal and vertical half-size decimation or interpolation and the clock frequency ratio. Horizontal decimation/interpolation operates on all color components for 4:2:2, 4:4:4 and 4:4:4:4 formats but the Y component only for 4:1:1(H4V1) and clearly for 4:0:0. There is no additional decimation/interpolation supported for 4:1:1 (H2V2). For half-size horizontal decimation/interpolation, filtering may be selected with the HRFL bit. Vertical decimation is a simple dropping of alternate lines and interpolation is done by replicating lines.

In compression the decimation is done only on the active window area and only after decimation is the data stored in the strip buffer. In expansion, any interpolation is done after reading data out of the strip buffer. Vertical interpolation is done by reading out the same line twice. The window area in expansion is specified after interpolation. Note carefully the minimum window areas for the different formats in Table 15.

Transfers with the ZR36050 are always at the SYSCLK clock rate, but as shown in the table, the PXCLK rate can sometimes be at one-half or one-quarter this rate. There is a choice of PXCLK to SYSCLK rate ratio for half-size horizontal, by the CKRT bit. Note, however, that the maximum PXCLK rate is limited to 15 MHz when color space conversion is used, so selecting a higher PXCLK to SYSCLK ratio generally implies reducing the frequency of SYSCLK rather than increasing the frequency of PXCLK.

Note that in Table 15 the Compressed Format and Resolution is after decimation in compression or before interpolation in expansion. The ZR36050 Image Format is as defined by the Mode Register, before decimation in compression or after interpolation in expansion.

Table 14: Operational Decimation/Interpolation Modes

ZR36050 Image Format	Decimation./Interpolation [1]			
	Full-Screen	Horizontal Half-Screen	Vertical Half-Screen	Quarter-Screen
4:2:2	◆	◆	◆	◆
4:1:1 (H4V1)	◆	◆	◆	◆
4:1:1 (H2V2)	◆	X	X	X
4:4:4	◆	◆	◆	◆
4:4:4:4	◆	◆	◆	◆
4:0:0	◆	◆	◆	◆

1. ◆ = Compressed picture size supported; X = size not supported in this image format.

Table 15: Decimation And Interpolation

ZR36050 Image Format	HORZ			VERT	Compression Format and Resolution	Minimum Value		PXCLK to SYSCLK Frequency Ratio	
	Bit	Decimation/ Interpolation [1]				PAX	PAY	CKRT	
		Y	CB/CR					0	1
4:2:2	1	◆	◆	1	2:1:1 (Quarter Screen)	32	16	1/2	1
4:2:2	1	◆	◆	0	2:1:1 (Horizontal Half-Screen)	32	8	1/2	1
4:2:2	0	–	–	1	4:2:2 (Vertical Half-Screen)	16	16	1/2	
4:2:2	0	–	–	0	4:2:2 (Full-Screen)	16	8	1/2	
4:1:1 (H4V1)	1	◆	–	1	2:1:1 (Quarter Screen)	32	16	1/2	1
4:1:1 (H4V1)	1	◆	–	0	2:1:1 (Horizontal Half-Screen)	32	8	1/2	1
4:1:1 (H4V1)	0	–	–	1	4:1:1 (Vertical Half-Screen)	32	16	1/2	
4:1:1 (H4V1)	0	–	–	0	4:1:1 (Full-Screen)	32	8	1/2	
4:1:1 (H2V2)	–	–	–	–	4:1:1 (Full-Screen)	16	16	1/2	
4:4:4	1	Each Component		1	2:2:2 (Quarter Screen)	16	16	1/4	1/2
4:4:4	1	Each Component		0	2:2:2 (Horizontal Half-Screen)	16	8	1/4	1/2
4:4:4	0	–	–	1	4:4:4 (Vertical Half-Screen)	8	16	1/4	
4:4:4	0	–	–	0	4:4:4 (Full-Screen)	8	8	1/4	
4:4:4:4	1	Each Component		1	2:2:2:2 (Quarter Screen)	16	16	1/2	1
4:4:4:4	1	Each Component		0	2:2:2:2 (Horizontal Half-Screen)	16	8	1/2	1
4:4:4:4	0	–	–	1	4:4:4:4 (Vertical Half-Screen)	8	16	1/2	
4:4:4:4	0	–	–	0	4:4:4:4 (Full-Screen)	8	8	1/2	
4:0:0 (1:0:0)	1	◆	–	1	2:0:0 (Quarter Screen)	16	16	1	
4:0:0 (1:0:0)	1	◆	–	0	2:0:0 (Horizontal Half-Screen)	16	8	1	
4:0:0 (1:0:0)	0	–	–	1	4:0:0 (Vertical Half-Screen)	8	16	1	
4:0:0 (1:0:0)	0	–	–	0	4:0:0 (Full-Screen)	8	8	1	

1. ◆ = Decimation/Interpolation is performed on these components; – = Not performed or not applicable.

Table 16 shows with shaded boxes which samples are dropped or reconstructed respectively by the horizontal decimation or interpolation process, for the various formats when HORZ = 1. When filtering is selected with the HRFL bit, the value at time n is [Y(n-1) + 2Y(n) + Y(n+1)]/4 on compression and is [Y(n-1) + Y(n+1]/2 on expansion. When n is at the edge of a window, Y(n) is copied and used for Y(n-1) or Y(n+1) as appropriate.

Table 16: The Horizontal Decimation/Interpolation

4:0:0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
4:4:4	R	R	R	R	R	R	R	R
	G	G	G	G	G	G	G	G
	B	B	B	B	B	B	B	B
4:4:4:4	Y	C	Y	C	Y	C	Y	C
	M	K	M	K	M	K	M	K
4:2:2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
4:1:1 (H4V1)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
	Cb0/Cr0				Cb4/Cr4			

Figure 12 illustrates a typical case of data flow, from the PXIN bus at the top through to the strip buffer, for an RGB input with color space conversion to YCbCr and horizontal decimation, with CKRT=1.

In this example, the internal pipeline delays of the various processing stages are ignored. The example is also intended to clarify the SYSCLK to PXCLK relationship. The strip buffer is always operated at a rate of half the SYSCLK frequency. When horizontal decimation is performed and CKRT=1, as in the above example, the PXCLK rate (and the PXIN pixel rate) is the same as that of SYSCLK. If horizontal decimation had not been selected, or if CKRT=0, the PXCLK rate would have been half the SYSCLK rate, the same as the strip buffer access rate.

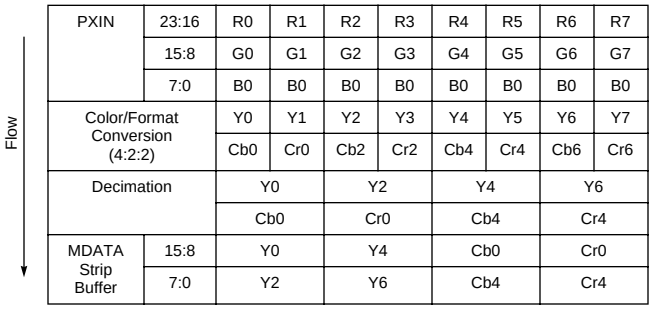


Figure 12. Typ. Data Flow from PXIN Bus to Strip Buffer

Mathematical Expressions For Color Space Conversions and Decimation/Interpolation (Format Conversion)

Expression of RGB toYC4:4:4 Conversion

- 8-bit Full-scale (CCIR = 0)

$$Yxx = 0.299Rxx + 0.587Gxx + 0.11Bxx$$
$$Crxx = 0.713\,(Rxx - Yxx)$$
$$Cbxx = 0.564\,(Bxx - Yxx)$$

- CCIR Standard (CCIR = 1)

$$Yxx = 0.299Rxx + 0.587Gxx + 0.11Bxx$$
$$Crxx = 0.729\,(Rxx - Yxx)$$
$$Cbxx = 0.577\,(Bxx - Yxx)$$

Expression of YC4:4:4 to YC4:2:2 Conversion

- Simple Decimation (SBFL = 0)

$$Yxx = Yxx$$
$$Crxx = Crxx$$
$$Cbxx = Cbxx$$

- Filter (SBFL = 1)

$$Yxx = Yxx$$
$$Crxx = \frac{Crx\,(x-1) + 2Crxx + Crx\,(x+1)}{4}$$
$$Cbxx = \frac{Cbx\,(x-1) + 2Cbxx + Cbx\,(x+1)}{4}$$

Expression of YC4:2:2 toYC4:1:1(H2V2) Conversion (vertical decimation only, no horizontal)

- Simple Decimation (SBFL = 0 or 1)

$$Yxx = Yxx$$
$$Crxx = Crxx$$
$$Cbxx = Cbxx$$

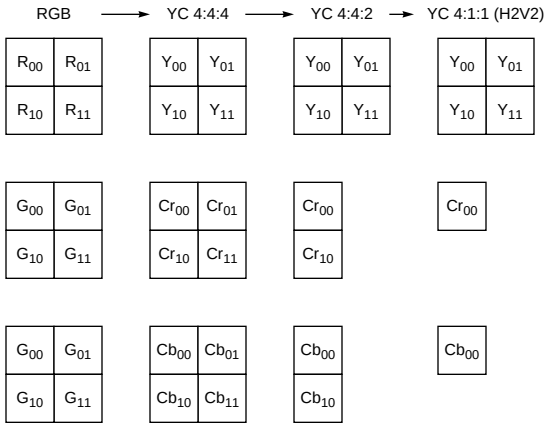


Figure 13. Decimation Flow

Expression of YC4:1:1(H2V2) to YC4:2:2 Conversion (Vertical interpolation only)

- Simple Interpolation (SBFL = 0 or 1)

$$Yxx = Yxx$$
$$Crxx = Crxx,\ Cr\,(x+1)\,x = Crxx$$
$$Cbxx = Cbxx,\ Cb\,(x+1)\,x = Cbxx$$

Expression of YC4:2:2 to YC4:4:4 Conversion

- Simple Interpolation (SBFL = 0)

$$Yxx = Yxx$$
$$Crxx = Crxx,\ Crx\,(x+1) = Crxx$$
$$Cbxx = Cbxx,\ Cbx\,(x+1) = Cbxx$$

- Filter (SBFL = 1)

$$Yxx = Yxx$$
$$Crx\,(x+1) = \frac{Crxx + Crx\,(x+2)}{2}$$
$$Cbx\,(x+1) = \frac{Cbxx + Cbx\,(x+2)}{2}$$

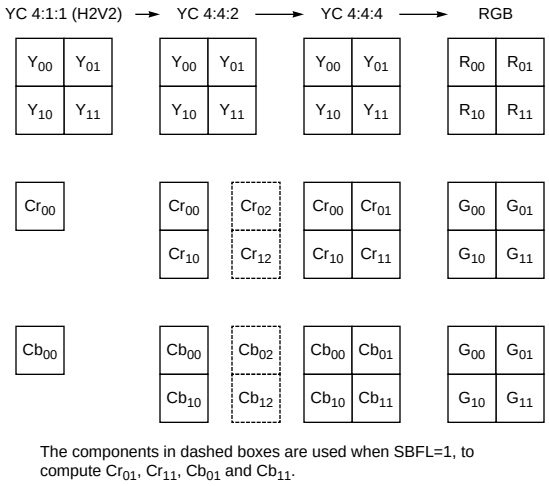
Expression of YC4:4:4 to RGB Conversion

- 8-bit Full-scale (CCIR = 0)

$$Rxx = Yxx + 1.37Crxx$$
$$Gxx = Yxx - 0.714Crxx - 0.344Cbxx$$
$$Bxx = Yxx + 1.772Cbxx$$

- CCIR Standard (CCIR = 1)

$$Rxx = Yxx + 1.37Crxx$$
$$Gxx = Yxx - 0.698Crxx - 0.336Cbxx$$
$$Bxx = Yxx + 1.73Cbxx$$



The components in dashed boxes are used when SBFL=1, to compute Cr_{01}, Cr_{11}, Cb_{01} and Cb_{11}.

Figure 14. Interpolation Flow

Compression/Expansion

Data Interfaces

The primary data flows are shown in Figure 15 for the compression and expansion modes. In compression data can be input on PXIN and be converted and output on PXOUT while also sending converted data within a window to the ZR36050 for compression.

For incoming data on PXIN the start of each frame is indicated by the rising edge of VIN and the start of each line is indicated by the rising edge of HIN. The active window area for ZR36016 processing starts on line NAY and on pixel NAX on that line. The processing continues for the window area of PAY lines and PAX pixels. An end of scan signal $\overline{EOS}$ is sent to the ZR36050 after the last pixel in the window is sent on compression. Similarly an $\overline{EOS}$ is expected from the ZR36050 on expansion.

Data going directly from PXIN to PXOUT can not be windowed. It can, however, undergo color space conversion and format conversion as determined by the MODE and DSPY fields, and filtering during the format conversion if the DSFL bit is set. The data is output with VOUT and HOUT after the internal processing delay.

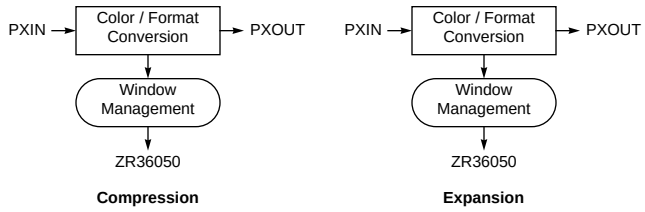


Figure 15. Data Flows Between PXIN, PXOUT and ZR36050

In expansion, the path from PXIN to PXOUT is the same as in compression. If there is expanded data from the ZR36050 it is overlayed in the window area as shown in Figure 16. Processing is again determined by the MODE and DSPY fields and by the DSFL bit.

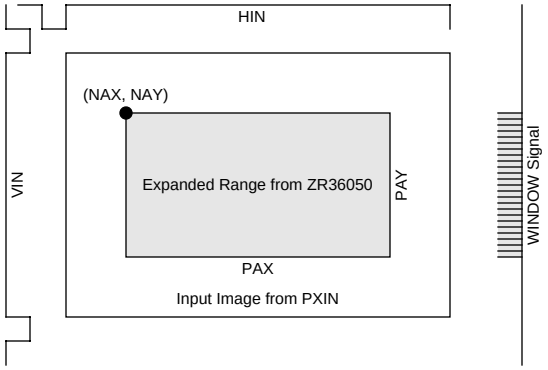


Figure 16. Overlay of Expanded Image on PXIN

Data on the PXIN and PXOUT buses are transferred with PXCLK which has the relationship to the system clock SYSCLK as shown in Table 8. PXIN, VIN and HIN are clocked with PXCLK on input and PXOUT, VOUT, HOUT and WINDOW are clocked with PXCLK on output.

Figure 17 shows the normal processing area in compression when the value of PAY is known (a non-zero value in the PAY register) and how WINDOW is active during the processing. Note where the end of scan signal $\overline{EOS}$ is generated.

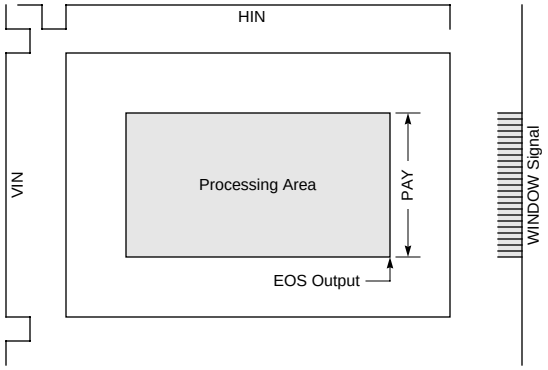


Figure 17. Normal Processing Area When PAY ≠ 0

Figure 18 shows the processing area in compression when PAY = 0, with the number of processed lines in a single frame unknown and determined by the falling edge of VIN.

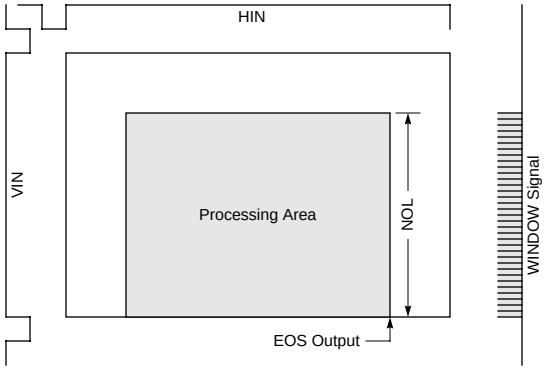


Figure 18. Processing Area When PAY = 0

The ZR36016 counts the number of lines in the processing range and enters this in the NOL (Number Of Lines) register. If the number of lines is not a multiple of 8 or 16, depending upon the format as shown in Table 15, then the number is corrected to be a proper multiple and entered in the register. When RSTR=1, the number of lines need not be a multiple of 8 or 16. If a VIN rising edge is not encountered after 64K lines, processing is terminated with NOL=64K.

GO/STOP Register and the START Signal

The GO/STOP register enables processing by the ZR36016 and terminates it, but it is the START signal in concert with STOP/GO that determines which VIN will be recognized and its associated data compressed, and which VIN will be recognized and trigger data output in expansion. The figures below show two examples for single frame mode, where a single frame is processed. Figure 19 is when START is held high and the control is accomplished with the GO/STOP register. Figure 20 shows control with the START signal after the register has been set. The timing of FBSY is for compression, with the end of scan signal $\overline{EOS}$ being output from the ZR36016 to the ZR36050. In both cases, the GO/STOP register will be cleared after processing a single frame and it must be re-enabled to begin processing the next frame.

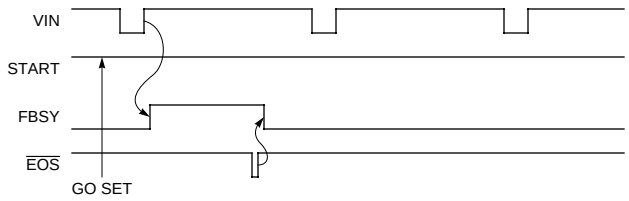


Figure 19. Processing Controlled by GO/STOP Register in Single Frame Compression Mode (CNTI = 0)

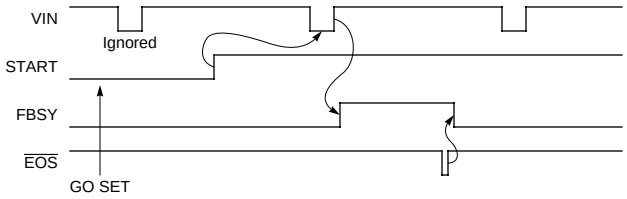


Figure 20. Processing Controlled by START Signal in Single Frame Compression Mode

Figures 21 and 22 show compression operation in sequential mode, with control by START and the GO/STOP register.

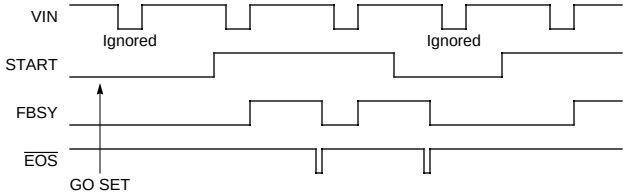


Figure 21. Sequential Mode Operation (CNTI = 1) with START Control

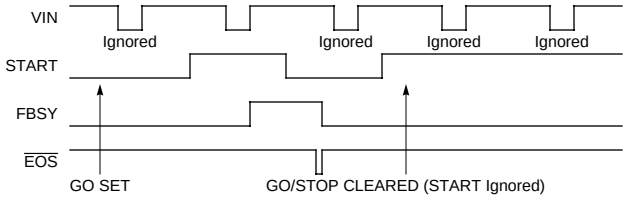


Figure 22. Sequential Mode Operation with GO/STOP Control

GO/STOP, START And FBSY Timing

When compressing, processing will start at the rising edge of VIN, if both the GO/STOP register is set and START is high before the rising edge of VIN. The time A shown in Figure 23 below must be greater than 0 in compression. In expansion, the time A must be sufficient to allow the first strip of the image (the minimum number of PAY lines, either 8 or 16 as shown in Table 19) to be read in from the ZR36050 and stored in the strip buffer. If the VIN rising edge occurs before the strip has been completely expanded by the ZR36050 and loaded in the strip buffer, either after the first GO (or START) or after completion of the previous image in sequential mode, the VIN will be ignored and the image will be output after the next VIN rising edge. In case of images that were compressed as interlaced fields, care must be taken to avoid mis-registration of fields.

During compression FBSY goes high at the rising edge of VIN and goes low after the active window has been processed.

During expansion FBSY goes high when the first $\overline{\text{DSYNC}}$ pulse from the ZR36050 is detected and goes low after the active window has been processed. WINDOW is active whenever data in the active window is being output, and when it is not active the PXIN image data is passed through to the PXOUT bus. These are illustrated below.

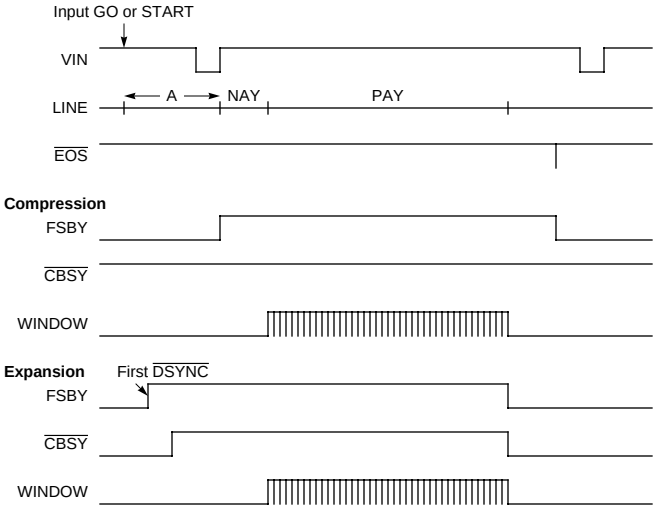


Figure 23. GO/STOP and START Timing for Compression and Expansion

$\overline{\text{CBSY}}$ Timing

Codec busy, $\overline{\text{CBSY}}$, is a signal output from the ZR36016 showing the state of transfers between the ZR36016 strip buffers and the ZR36050. It indicates that the strip buffer on the ZR36050 side is still busy when the strip buffer on the pixel side becomes available and the buffers can not be exchanged. If the buffer exchange does not occur before the rising edge of HIN, the data of that line will be lost during compression, and during expansion the line will not contain expanded data and PXIN data will be substituted.

If $\overline{\text{CBSY}}$ becomes active but is then cleared when the ZR36050-side strip buffer becomes ready, normal operation will continue on the next rising edge of HIN. However if PAX < 24 then there must be 16 clock periods of PXCLK before the rising edge of HIN to insure normal operation.

$\overline{\text{CBSY}}$ Timing On Compression

After the last pixel of the PAX portion of the last buffer line has been input on PXIN and sent to the strip buffer, a check is made to see that the previous buffer has been completely read out to the ZR36050. If it has not, then $\overline{\text{CBSY}}$ is asserted. Figure 24 shows a case where the previous buffer is ready immediately and $\overline{\text{CBSY}}$ is not asserted.

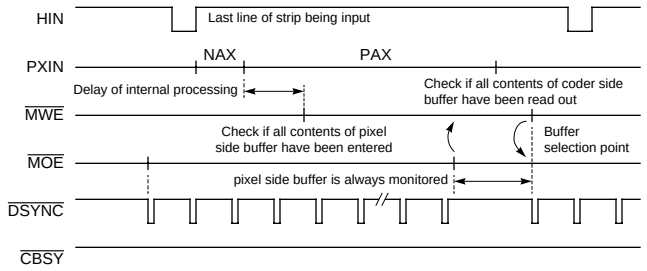


Figure 24. Normal Compression Operation when $\overline{\text{CBSY}}$ is Not Asserted

Figure 25 shows the condition where $\overline{\text{CBSY}}$ is asserted but the line is not ignored.

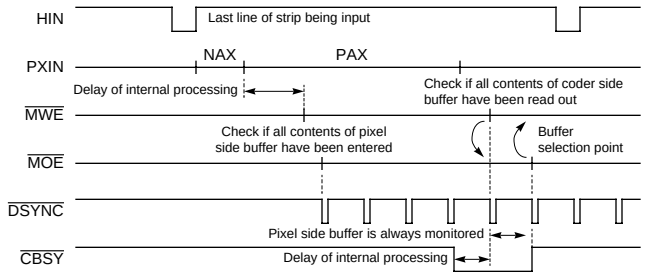


Figure 25. Compression Operation When $\overline{\text{CBSY}}$ is Asserted but the Line is not Ignored

Figure 26 shows the case where $\overline{\text{CBSY}}$ is asserted and a line is ignored. $\overline{\text{CBSY}}$ becomes active on line 8n. Processing of line 8n is completed in the ZR36016 and line 8n+1 will be ignored. At the next rising edge of HIN, if $\overline{\text{CBSY}}$ is not asserted, the processing is restarted (with line 8n+2).

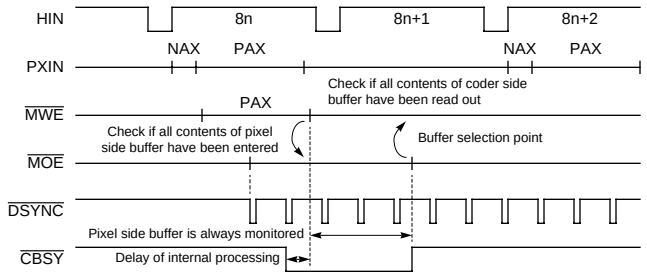


Figure 26. Compression Operation when $\overline{\text{CBSY}}$ is Asserted and A Line is Ignored

$\overline{\text{CBSY}}$ Timing On Expansion

$\overline{\text{CBSY}}$ is asserted immediately after GO/STOP is set and CMPR = 0. It remains asserted while the ZR36050 is filling the first buffer and PXIN data is being output on the PXOUT bus. Normal operation then proceeds as shown in Figure 27 where $\overline{\text{CBSY}}$ is not asserted.

When the last pixel of the PAX portion of the last buffer line is output on the PXOUT bus, a check is made to see if the next buffer has been loaded from the ZR36050 (8 or 16 lines if RSTR = 0 or one line if RSTR = 1). If it has not been loaded, then $\overline{CBSY}$ is asserted.

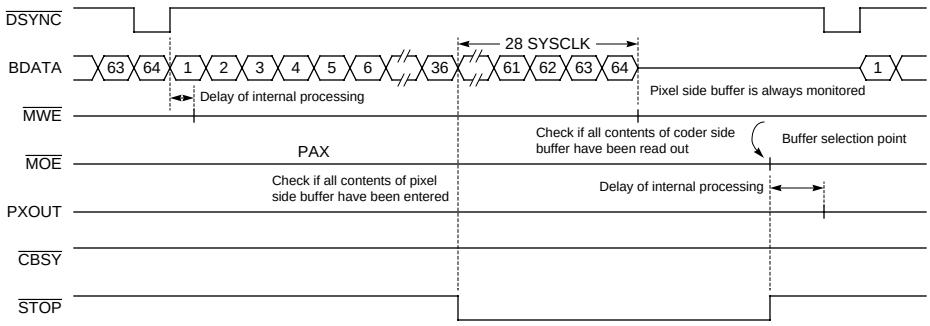


Figure 27. Normal Expansion Operation When CBSY is Not Asserted

Figure 28 shows the condition when $\overline{CBSY}$ is asserted but the line is not ignored. However, if $\overline{CBSY}$ is asserted at the time HIN rises, the expansion process on the next line is ignored and the image data coming from PXIN is output from PXOUT instead.

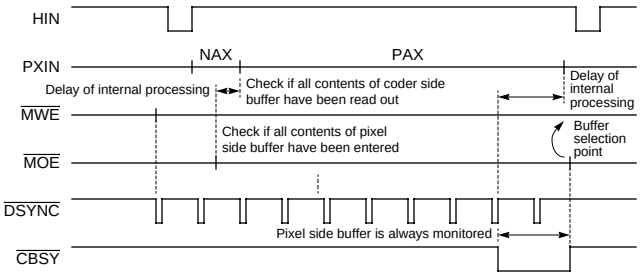


Figure 28. Expansion Operation When $\overline{CBSY}$ is Asserted but the Line is Not Ignored

Strip Buffer And Sub-Buffer

The external strip buffer memory is used for the raster-to-block and block-to-raster conversions. Double buffering is used for the 8 or 16 lines per block or a single line for raster-to-raster conversion. The memory is typically composed of two physical 8-bit-wide memories organized as shown in Figure 29. A/B and A'/B' are the two strip buffers. Reading and writing are always done with 16-bit accesses. The switch between reading and writing takes place at the SYSCLK rate. The sub-buffer allows continuous pixel data flow while the ZR36050-side buffer is being accessed.

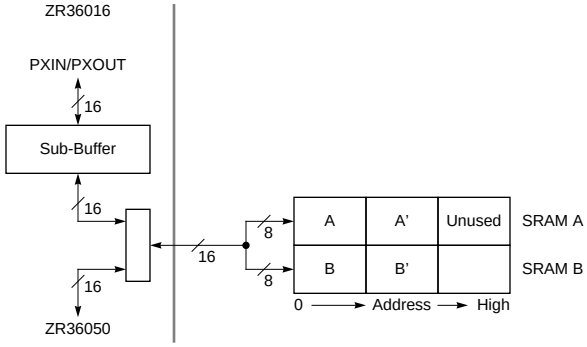


Figure 29. Strip Buffer Interface

Size of External Strip Memory

The minimum required size in bytes of the strip memory for each format is:

Size = 2 x K x L x PAX x D bytes

where values of K and L are determined from Table 17. D = 1 when HORZ = 0 and D = 0.5 when HORZ = 1. D = 1 always for the 4:1:1 (H2V2) format. When RSTR = 1, L = 1 in any format.

Table 17: Calculation Parameters For Strip Memory

	ZR36050 Image Format					
Coef	**1:0:0**	**4:2:2**	**4:1:1 (H2V2)**	**4:1:1 (H4V1)**	**4:4:4**	**4:4:4:4**
K	1	2	1.5	1.5 [1]	3	4
L	8	8	16	8	8	8

1. K = 2 when HORZ = 1.

Limitations on the value of PAX are given in Table 18.

Table 18: Limitations on PAX

RSTR Bit	HORZ	PAX	ZR36050					
			1:0:0	4:2:2	4:1:1 (H2V2)	4:1:1 (H4V1)	4:4:4	4:4:4:4
0	0	Max Value	8192	4096	2720	5440	2728	2048
		Min Value	8	16	16	32	8	8
		Multiple of…	8	16	16	32	8	8
	1	Max Value	16348	8192		8192	5456	4096
		Min Value	16	32		32	16	16
		Multiple of…	16	32		32	16	16
1	0	Max Value	65536	32768		43688	21840	16348
		Min Value	8	8		8	8	8
		Multiple of…	8	8		8	8	8
	1	Max Value	65536	65536		65536	43688	32768
		Min Value	16	16		16	16	16
		Multiple of…	16	16		16	16	16

The limitations on PAY when RSTR = 0 are in Table 19.

Table 19: Limitations on PAY

VERT Bit	PAY	ZR36050					
		1:0:0	4:2:2	4:1:1 (H2V2)	4:1:1 (H4V1)	4:4:4	4:4:4:4
0	Max Value	65536	65536	65536	65536	65536	65536
	Min Value	8	8	16	8	8	8
	Multiple of…	8	8	16	8	8	8
1	Max Value	65536	65536		65536	65536	65536
	Min Value	16	16		16	16	16
	Multiple of…	16	16		16	16	16

In the case of RSTR = 1, the maximum value of PAY is 65536 in any format. The minimum value is 1 when VERT = 0 and is 2 when VERT = 1.

ZR36050 Bus Interface

The ZR36016 connects directly with the ZR36050 as shown in Figure 30. The data transfer rate on BDATA(7:0) is always at the SYSCLK clock rate regardless of the format.

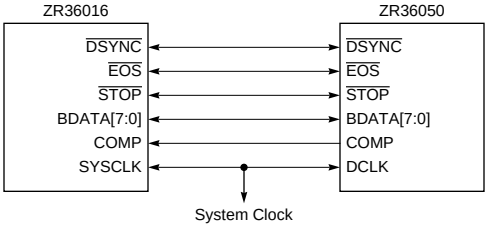


Figure 30. ZR36016 to ZR36050 Connections

The direction of the bidirectional pins on the ZR36016, and therefore possible transfers, is determined by the COMP input signal from the ZR36050 rather than the CMPR bit of the Mode register in the ZR36016. These two conditions are shown in Table 20.

If the ZR36016 is set for compression in the Mode register and receives a low input on COMP indicating expansion it will output an active $\overline{\text{STOP}}$ provided it is not already processing.

Table 20: Directional Status of ZR36016 Pins on the ZR36050 Interface

Pin	Compression	Expansion
COMP	IN High	IN Low
$\overline{\text{DSYNC}}$	OUT	INT
$\overline{\text{EOS}}$	OUT	IN
$\overline{\text{STOP}}$	IN	OUT
BDATA(7:0)	OUT	IN

For transfers with the ZR36050 the $\overline{\text{DSYNC}}$ signal is treated as a pixel enable when RSTR = 1 for raster-to-raster transfers rather than as a block enable for block transfers. See the ZR36050 User's Manual for its timing information.

JPEG MCU (Minimum Coded Unit) Structure

Data transfer between the ZR36016 and the ZR36050 is always in units of the MCU. The structure of the MCU for each of the supported compressed data formats is shown in Table 21. For baseline compression, the entities of the MCU are 8x8 blocks; for lossless and fast preview, they are individual samples.

Table 21: MCU Structure

ZR36050 Image Format	MCU Structure	
4:2:2	Y0 Y1 Cb0 Cr0	Y0, Y1, Cb0, Cr0
4:1:1 (H4V1)	Y0 Y1 Y2 Y3 Cb0 Cr0	Y0, Y1, Y2, Y3, Cb0, Cr0
4:1:1 (H2V2)	Y0 Y1 / Y2 Y3 Cb0 Cr0	Y0, Y1, Y2, Y3, Cb0, Cr0
4:4:4	R0 G0 B0	R0, G0, B0
4:4:4:4	C0 M0 Y0 K0	C0, M0, Y0, K0
4:0:0	Y0	Y0

Example Functional Timing Diagrams for Baseline Compression (Raster-to-Block Conversion)

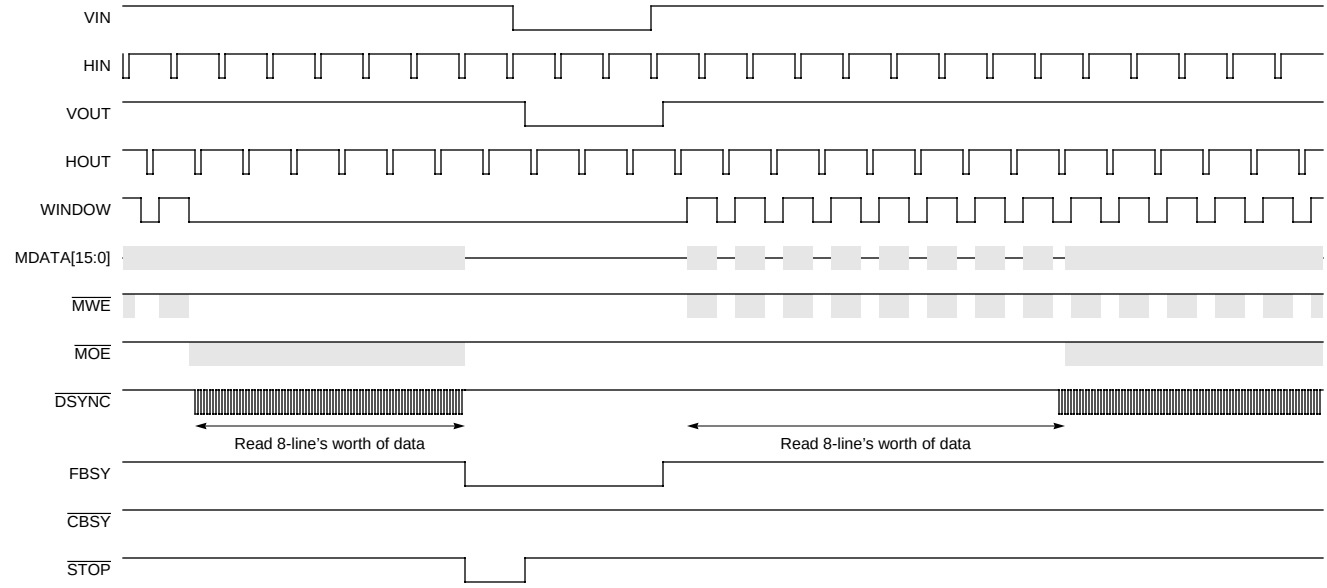


Figure 31. Functional Timing Diagram for Compression

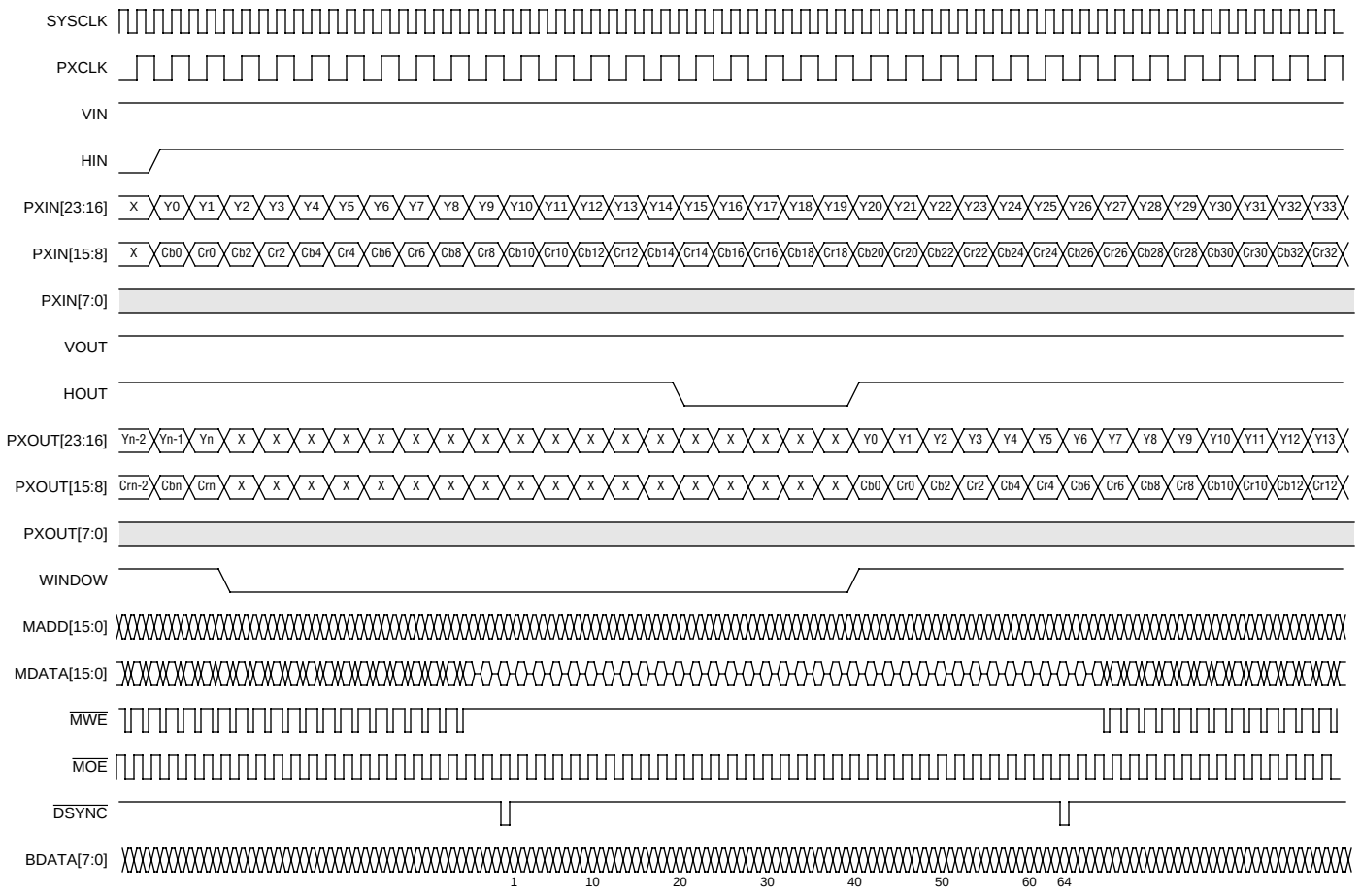


Figure 32. Functional Timing Diagram for Compression, YCbCr 4:2:2, HORZ = 0, VERT = 0

Example Functional Timing Diagrams for Baseline Expansion (Block-to-Raster Conversion)

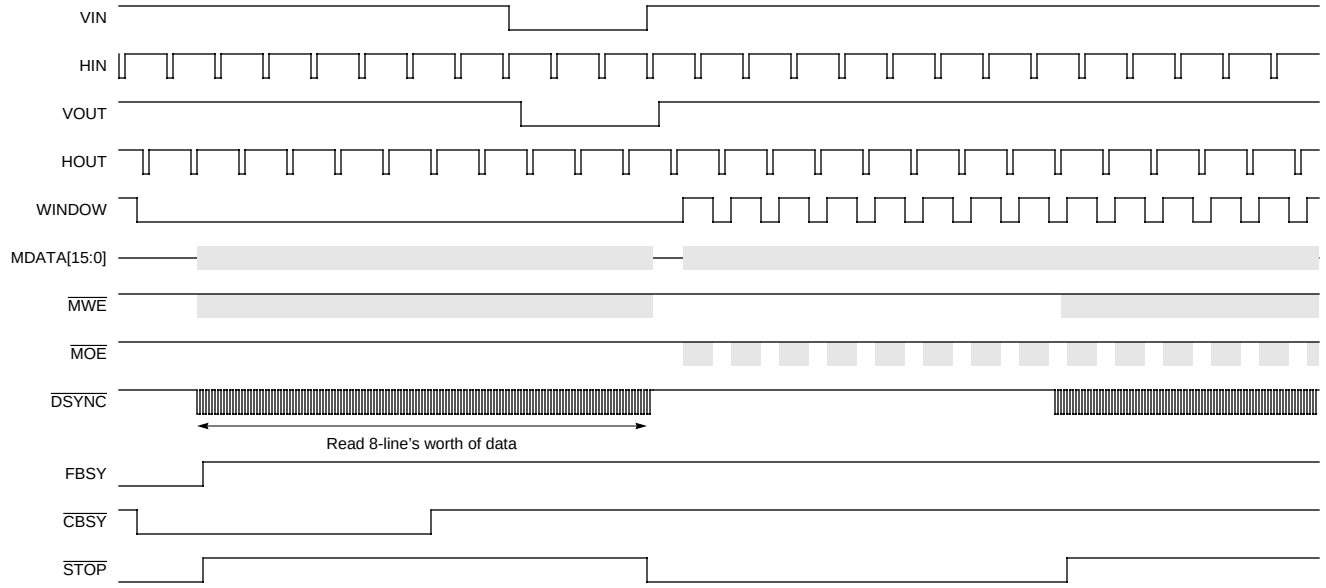


Figure 33. Functional Timing Diagram for Expansion

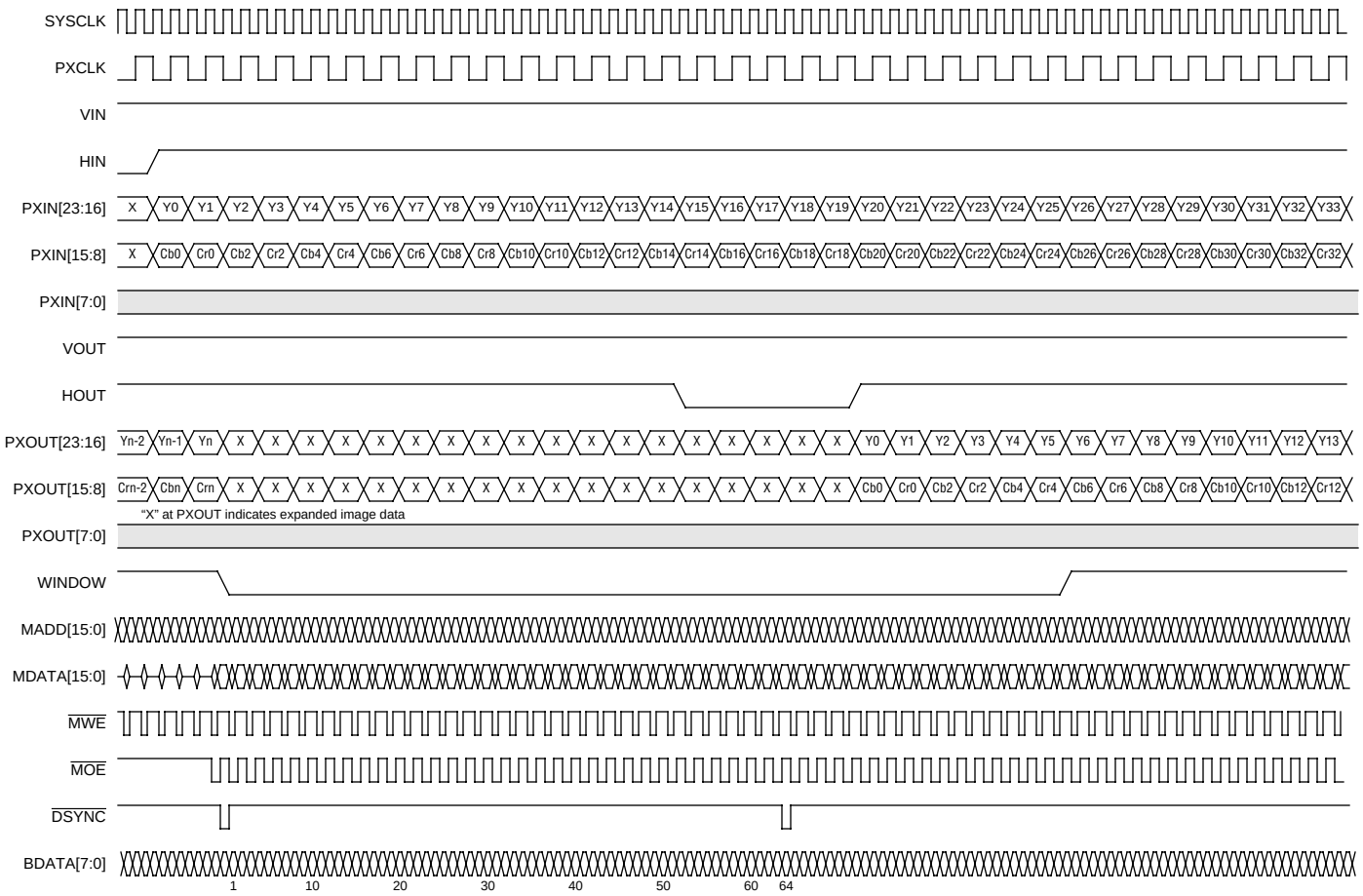


Figure 34. Functional Timing Diagram for Expansion, YCbCr 4:2:2, HORZ = 0, VERT = 0

Fast Preview Function

The Fast Preview function allows a compressed image to be expanded rapidly with 1/8-th resolution in both the horizontal and vertical directions. The expanded image is output on PXOUT from the point designated by NAX and NAY.

For Fast Preview, RSTR = 1.

Lossless Compression/Expansion

The ZR36016 supports the lossless compression/expansion function of the ZR36050. Note that the ZR36050 supports image data precision of 2-12 bits, but the ZR36016 supports only up to 8 bits.

For lossless operation, RSTR = 1.

A recommended Huffman table for 8-bit precision is:

ID = 0	
Length	0 1 5 1 1 1 0 0 0 0 0 0 0 0 0 0
Value	0 1 2 3 4 5 6 7 8

Host Interface

The Host Interface is used for the setting and reading of the internal control registers. The access to these control registers is permitted only when the ZR36016 is idle, or while FBSY is not asserted. The only exception is the GO/STOP register, which can be accessed at any time.

Register Access

Register access is asynchronous with the system clock SYSCLK. A typical transfer is shown in Figure 35.

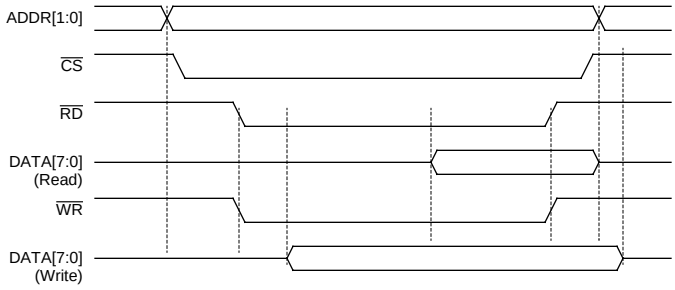


Figure 35. Control Register Access

The Frame Busy Signal FBSY

The following are the conditions when the Frame Busy signal is asserted or negated.

During Compression:

Asserted: After the VIN rising edge at the start of a frame which is subject to data processing.

Negated: After the ZR36016 outputs $\overline{EOS}$ to the ZR36050.

During Expansion:

Asserted: Immediately after GO is set or after receiving $\overline{DSYNC}$ from the ZR36050.

Negated: After $\overline{EOS}$ is received from the ZR36050 and all data has been output on PXOUT.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....-40°C to +125°C
Supply Voltage to Ground ..... -0.3V to +7.0V
DC Output Voltage .....-0.3V to VDD+0.3V
DC Input Voltage .....-0.3V to VDD+0.3V
DC Input Current, any single input .....-10 mA to +10 mA
DC Output Current, any single output ..... -20 mA to +20 mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above those limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Ambient Temperature.....0°C to +70°C
Supply Voltage .....4.75V to 5.25V

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 8 mA, $\overline{MWE}$ and $\overline{MOE}$ only
						I_{OL} = 16 mA, all other outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8 mA, $\overline{MWE}$ and $\overline{MOE}$ only
						I_{OH} = -16 mA, all other outputs
I_{LI}	Input Leakage Current			±20	µA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Output Leakage Current			±20	µA	$V_{OUT} = V_{CC}$ or GND, output disabled
I_{CC}	Power Supply Current		220		mA	V_{DD} = 5V, SYSCLK = 30 MHz, PXCLK = 15 MHz, C_L = 50pF, T_A = 25°C

AC CHARACTERISTICS

Clocks & Image Interface (Load Capacitance C_L = 50 pF)

Symbol	Parameter	Min	Typ	Max	Units
t_{CC}	Clock Cycle Time	33			ns
t_{CLH}	Clock “H” Time	14			ns
t_{CLL}	Clock “L” Time	14			ns
t_{CLS}	Clock Skew (SYSCLK-PXCLK)			10	ns
t_{PDS}	Pixel Data Setup Time	t_{CLS} + 2			ns
t_{PDH}	Pixel Data Hold Time	7 - t_{CLS}			ns
t_{SNCS}	HIN, VIN Setup Time	t_{CLS} + 10			ns
t_{SNCH}	HIN, VIN Hold Time	4			ns
t_{WDD}	Window Output Delay Time	7 - t_{CLS}		19	ns
t_{WDH}	Window Output Hold Time	2			ns
t_{PSD}	PXOUT, HOUT, VOUT Output Delay Time			26	ns
t_{PSH}	PXOUT, HOUT, VOUT Output Hold Time	2			ns
t_{PSOED}	PXOUT, HOUT, VOUT Output Delay Time from PXOE Rising Edge			19	ns
t_{PSOEH}	PXOUT, HOUT, VOUT Output Hold Time from PXOE Rising Edge	2			ns
t_{PES}	Pixel Enable Setup Time	4			ns
t_{PEH}	Pixel Enable Hold Time	2			ns
t_{RSS}	Reset Setup Time	4			ns
t_{RSH}	Reset Hold Time	2			ns
t_{BYD}	FBSY, CBSY Output Delay Time			23	ns
t_{BYH}	FBSY, CBSY Output Hold Time	2			ns

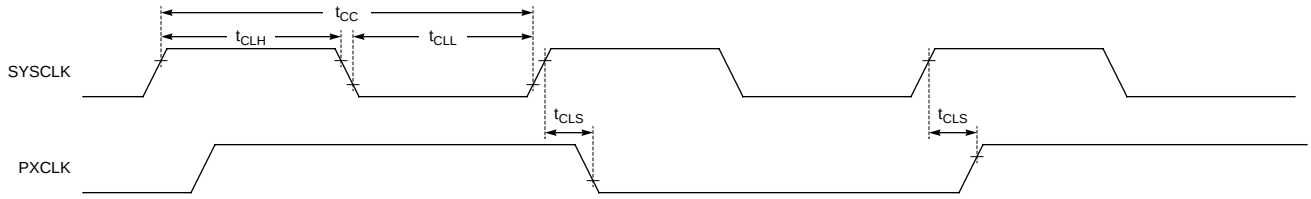


Figure 36. Clock Timing

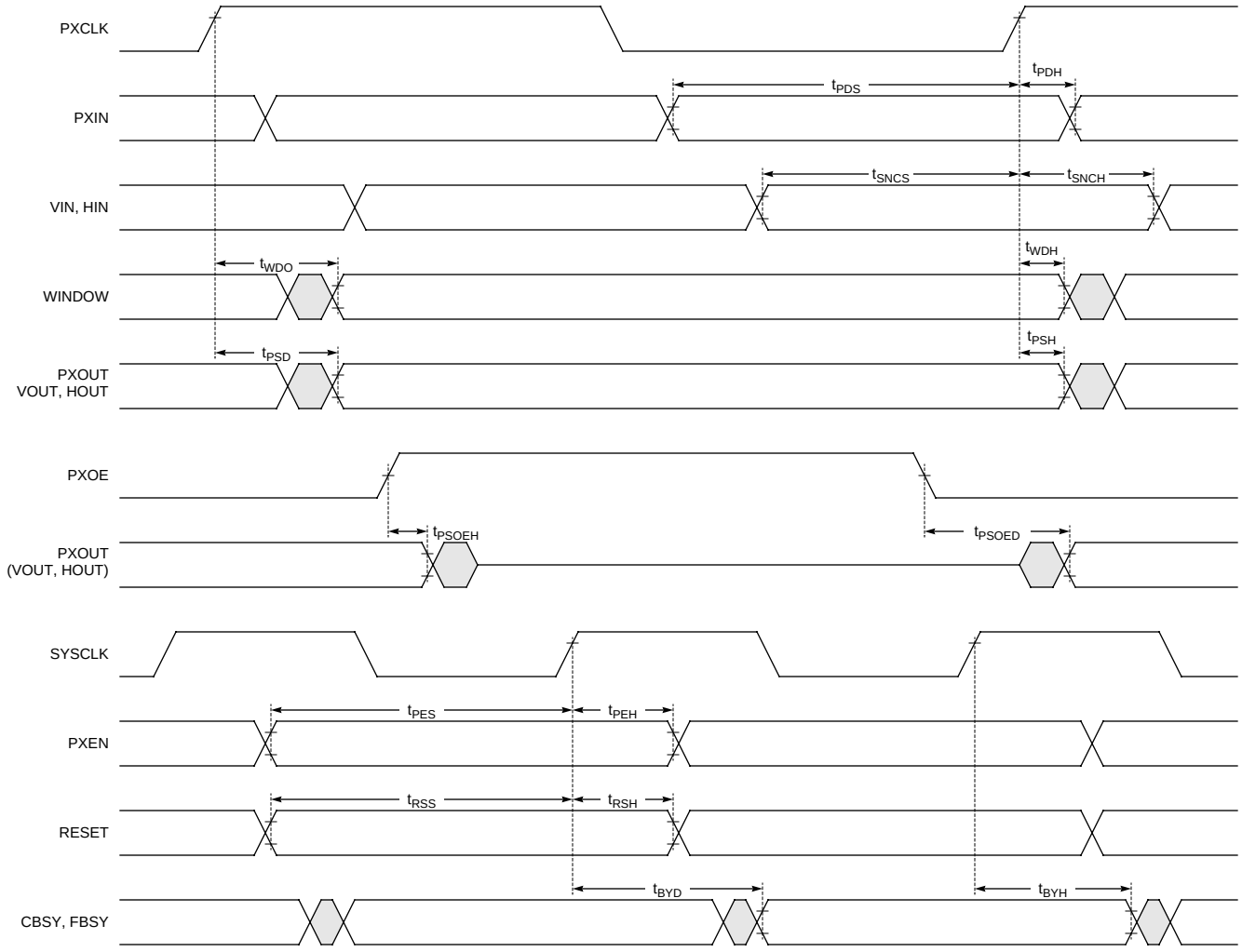


Figure 37. Image Interface Timing

CODEC Interface (Load Capacitance C_L = 20 pF)

Symbol	Parameter	Min	Typ	Max	Units
t_{CDS}	Data Setup Time	11			ns
t_{CDH}	Data Hold Time	2			ns
t_{CDOD}	Data Output Delay Time			14	ns
t_{CDOH}	Data Output Hold Time	4			ns
t_{CDCPD}	Data Output Delay Time (from COMP)			12	ns
t_{CDCPH}	Data Output Hold Time (from COMP)	1			ns

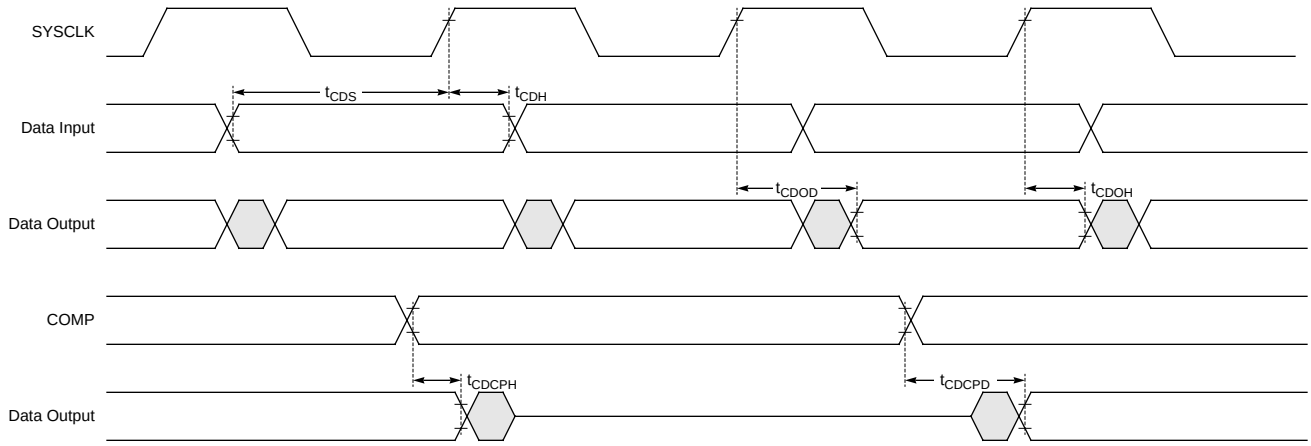


Figure 38. CODEC Interface Timing

Host Interface (Load Capacitance C_L = 50 pF)

Symbol	Parameter	Min	Typ	Max	Units
t_{CSS}	Chip Select Setup Time	0			ns
t_{CSH}	Chip Select Hold Time	0			ns
t_{RADS}	Read Address Setup TIme	7			ns
t_{RADH}	Read Address Hold Time	0			ns
t_{DTD}	Read/Write Pulse Width	20			ns
t_{DTH}	Read Data Output Delay Time			17	ns
t_{WRDS}	Read Data Output Hold Time	2			ns
t_{WRDH}	Write Data Setup Time	7			ns
t_{WADS}	Write Address Setup Time	0			ns
t_{WADH}	Write Address Hold Time	5			ns

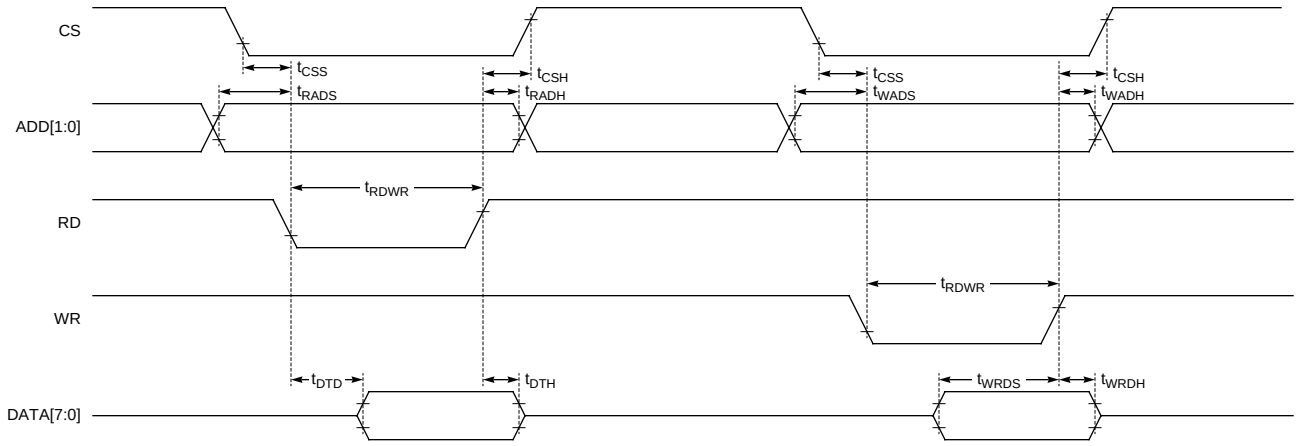


Figure 39. Host Interface Timing

Memory Interface (Load Capacitance C_L = 50 pF)

Symbol	Parameter	Min	Typ	Max	Units
t_{CSS}	Chip Select Setup Time	0			ns
t_{CSH}	Chip Select Hold Time	0			ns
t_{RADS}	Read Address Setup TIme	7			ns
t_{RADH}	Read Address Hold Time	0			ns
t_{DTD}	Read/Write Pulse Width	20			ns
t_{DTH}	Read Data Output Delay Time			17	ns
t_{WRDS}	Read Data Output Hold Time	2			ns
t_{WRDH}	Write Data Setup Time	7			ns
t_{WADS}	Write Address Setup Time	0			ns
t_{WADH}	Write Address Hold Time	5			ns

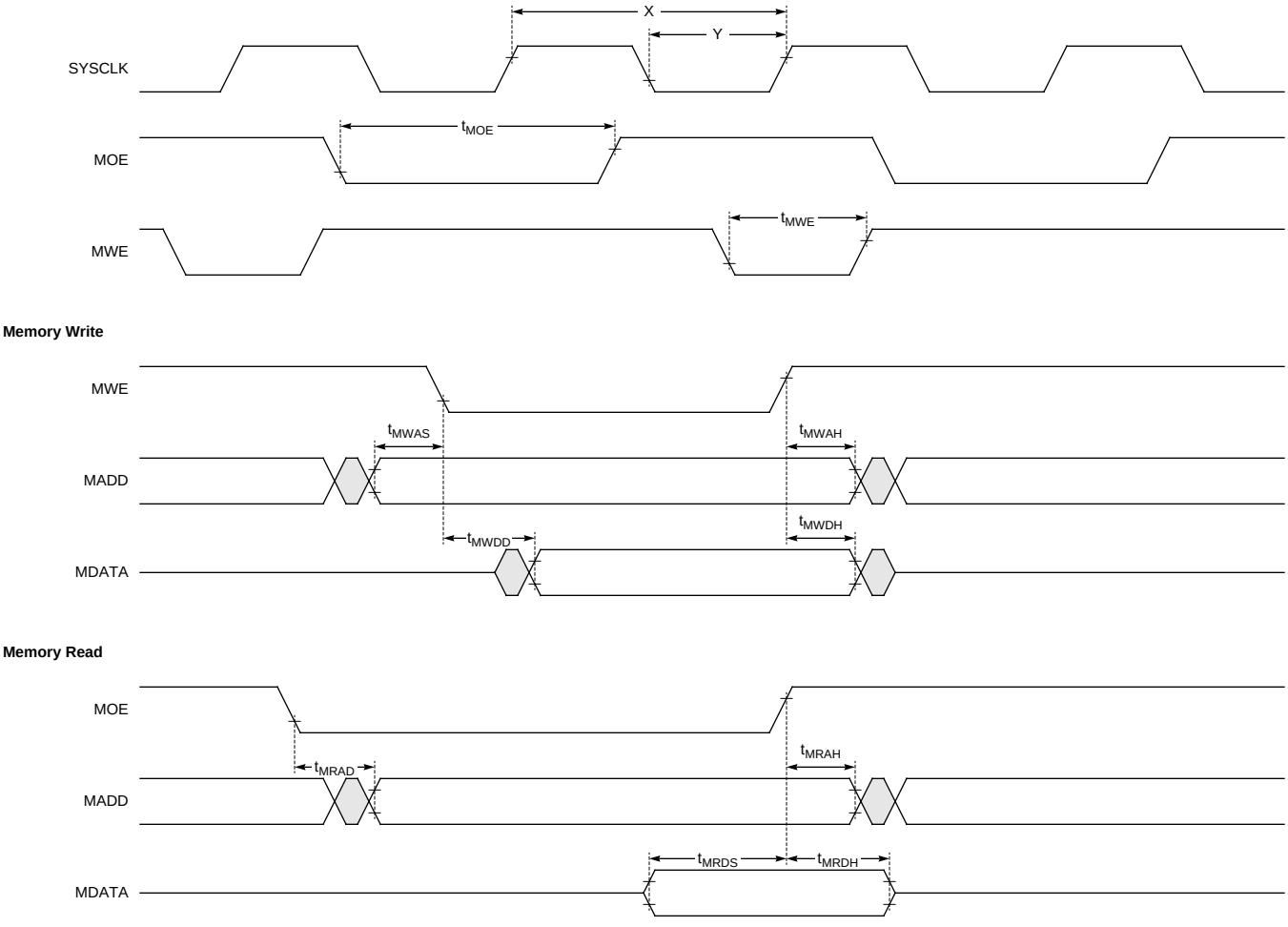


Figure 40. Memory Interface Timing

PACKAGE INFORMATION

160-Pin Quad Flat Pack Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	FBSY	21	SYSCLK	41	NC	61	GND	81	MDATA14	101	MDATA0	121	NC	141	PXIN9
2	DATA7	22	COMP	42	GND	62	PXOUT9	82	MDATA13	102	MADD15	122	MADD1	142	PXIN8
3	DATA6	23	$\overline{EOS}$	43	VOUT	63	PXOUT8	83	MDATA12	103	MADD14	123	MADD0	143	PXIN7
4	DATA5	24	$\overline{STOP}$	44	PXOUT23	64	PXOUT7	84	GND	104	MADD13	124	PXIN23	144	PXIN6
5	DATA4	25	$\overline{DSYNC}$	45	PXOUT22	65	PXOUT6	85	MDATA11	105	MADD12	125	PXIN22	145	PXIN5
6	NC	26	NC	46	PXOUT21	66	PXOUT5	86	NC	106	NC	126	PXIN21	146	PXIN4
7	GND	27	BDATA7	47	PXOUT20	67	PXOUT4	87	MDATA10	107	GND	127	PXIN20	147	PXIN3
8	VDD	28	GND	48	PXOUT19	68	PXOUT3	88	MDATA9	108	MADD11	128	PXIN19	148	PXIN2
9	DATA3	29	BDATA6	49	NC	69	PXOUT2	89	MDATA8	109	MADD10	129	NC	149	PXIN1
10	DATA2	30	BDATA5	50	GND	70	GND	90	MDATA7	110	MADD9	130	GND	150	GND
11	DATA1	31	BDATA4	51	PXOUT18	71	NC	91	MDATA6	111	MADD8	131	PXIN18	151	NC
12	DATA0	32	BDATA3	52	PXOUT17	72	PXOUT1	92	MDATA5	112	VDD	132	PXIN17	152	PXIN0
13	START	33	BDATA2	53	PXOUT16	73	NC	93	MDATA4	113	MADD7	133	PXIN16	153	NC
14	$\overline{RESET}$	34	VDD	54	VDD	74	PXOUT0	94	GND	114	MADD6	134	PXIN15	154	VIN
15	NC	35	BDATA1	55	PXOUT15	75	$\overline{PXOE}$	95	NC	115	MADD5	135	PXIN14	155	HIN
16	$\overline{PXEN}$	36	BDATA0	56	PXOUT14	76	GND	96	MDATA3	116	MADD4	136	PXIN13	156	$\overline{RD}$
17	TMODE	37	$\overline{CBSY}$	57	PXOUT13	77	VDD	97	MDATA2	117	GND	137	PXIN12	157	$\overline{WR}$
18	PXCLK	38	WINDOW	58	PXOUT12	78	$\overline{MWE}$	98	MDATA1	118	MADD3	138	PXIN11	158	$\overline{CS}$
19	GND	39	HOUT	59	PXOUT11	79	$\overline{MOE}$	99	GND	119	MADD2	139	PXIN10	159	ADD1
20	VDD	40	NC	60	PXOUT10	80	MDATA15	100	VDD	120	NC	140	VDD	160	ADD0

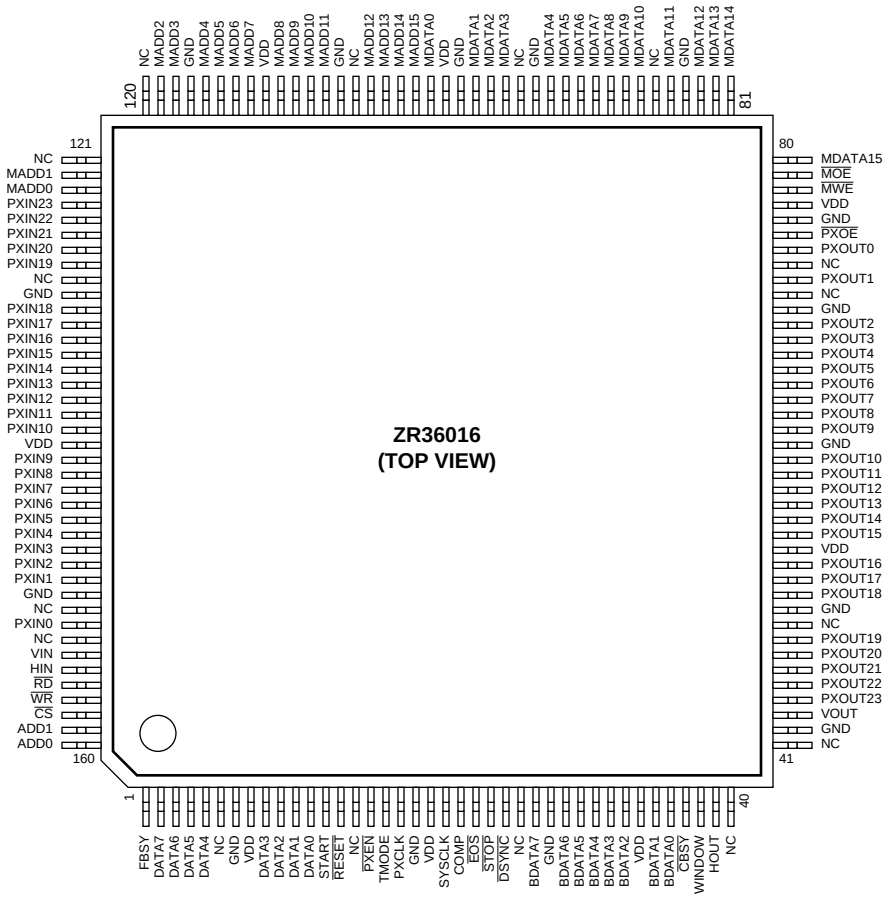
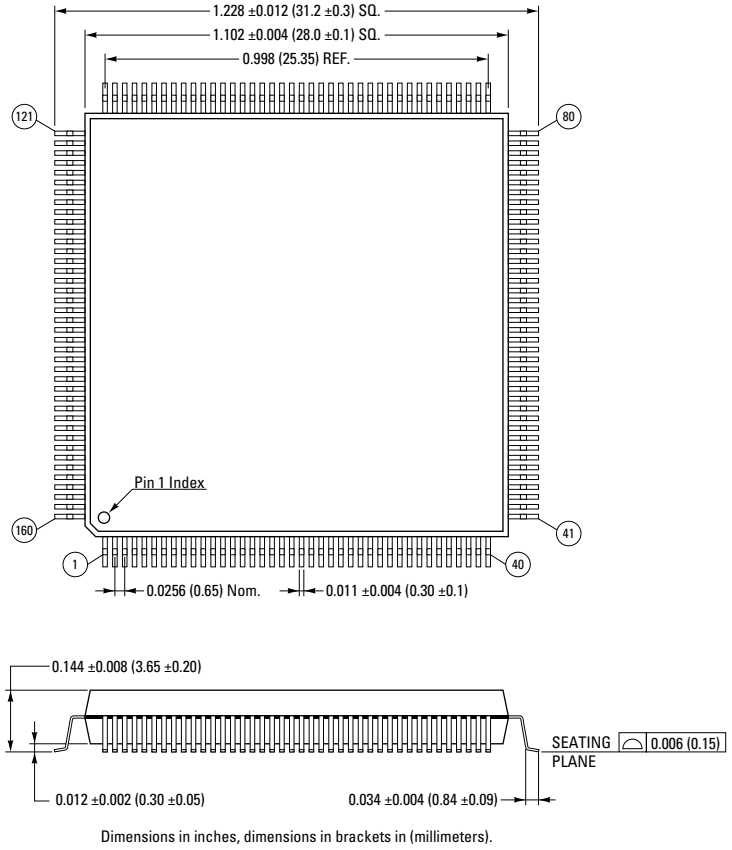


Figure 41. ZR36016 Plastic Quad Flat Pack Pinout

PACKAGE INFORMATION



Dimensions in inches, dimensions in brackets in (millimeters).

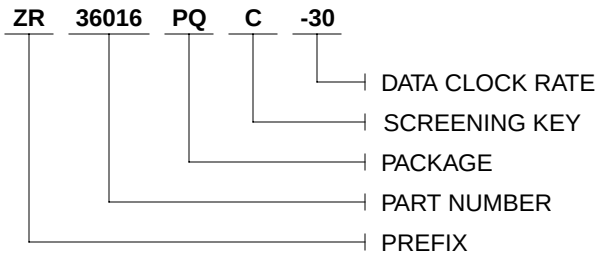
Figure 42. ZR36016 Plastic Quad Flat Pack Dimensions

Notes:

Notes:

Notes:

ORDERING INFORMATION



PACKAGE

PQ - Plastic Quad Flat Pack (EIAJ)

DATA CLOCK RATE

-30: 30 MHz

SCREENING KEY

C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)

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